(12)

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-266567
(43)Date of publication of application : 28.09.2001

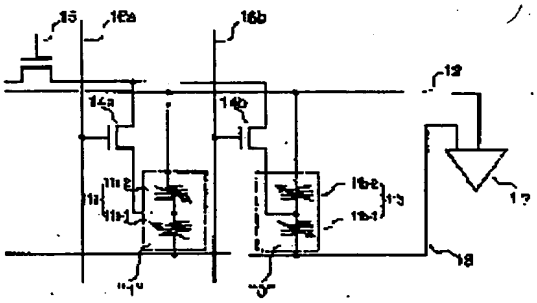
(51)Int.Cl. G11C 11/15
H01F 10/06
H01F 10/26
H01F 10/32
H01L 27/10
H01L 43/08

(21)Application number : 2000-075168
(22)Date of filing : 17.03.2000

(71)Applicant : TOSHIBA CORP
(72)Inventor : INOMATA KOICHIRO
NAKAJIMA KENTARO
SAITO YOSHIAKI

(54) MAGNETIC MEMORY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a new magnetic memory device having large signal voltage and large S/N and contributing to capacity enlargement.
SOLUTION: This device is provided with a first magnetizing fixed film, a first tunnel insulation film arranged closely to the first magnetizing fixed film, a first tunnel junction 11a-1 provided with a first ferromagnetic layer which is arranged opposing to the magnetizing fixed film through the first tunnel insulation film and in which a direction of magnetization is varied by an external magnetic field, a second tunnel junction 11a-2 provided with a second magnetizing layer in which a direction of magnetization is varied by an external magnetic field by coupling with the first ferromagnetic layer in an anti-ferromagnetic state, a second tunnel insulation film, and a second magnetizing fixed film which is arranged opposing to the second ferromagnetic layer through the second tunnel insulation film, always, either of the first tunnel junction and the second tunnel junction keeps low resistance and the other junction keeps high resistance. A read-out current is made to flow separately to the first tunnel junction and the second tunnel junction, and the current difference or difference of load voltage can be differential-detected by a sense amplifier 17.



LEGAL STATUS

[Date of request for examination] 02.08.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] The 1st ferromagnetism magnetization fixing film with which the magnetization direction was fixed, and the 1st tunnel insulator layer by which contiguity arrangement was carried out with said 1st ferromagnetism magnetization fixing film, Opposite arrangement is carried out with said 1st ferromagnetism magnetization fixing film through said 1st tunnel insulator layer. Antiferromagnetism association is carried out with the 1st magnetic layer which changes the sense of magnetization by the external magnetic field, and said 1st a little more than magnetic layer. The magnetic storage film equipped with the nonmagnetic conductive layer which it is arranged [conductive layer] between the 2nd magnetic layer which changes the sense of magnetization by said external magnetic field, said 1st [the], and the 2nd a little more than magnetic layer, and carries out antiferromagnetism association of said 1st and 2nd magnetic layers, The tunnel junction component which equips said magnetic storage film with the 2nd ferromagnetism magnetization fixing film by which opposite arrangement was carried out at said 2nd magnetic layer through the 2nd tunnel insulator layer by which contiguity arrangement was carried out, and said 2nd tunnel insulator layer, The magnetic memory apparatus characterized by having the 1st wiring which carries out electrical connection to said magnetic storage film, the 2nd wiring which carries out electrical connection to said 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to said 2nd ferromagnetism magnetization fixing film.
[Claim 2] The magnetic memory apparatus according to claim 1 characterized by detecting the current difference or load electrical-potential-difference difference of the 1st tunnel current which flows between said magnetic storage film and said 1st ferromagnetism magnetization fixing film, and the 2nd tunnel current which flows between said magnetic storage film and said 2nd ferromagnetism magnetization fixing film by the differential method.
[Claim 3] The 1st ferromagnetism magnetization fixing film with which the magnetization direction was fixed, and the 1st tunnel insulator layer by which contiguity arrangement was carried out with said 1st magnetic film, Opposite arrangement is carried out with said 1st ferromagnetism magnetization fixing film through said 1st tunnel insulator layer. Antiferromagnetism association is carried out with the 1st magnetic layer which changes the sense of magnetization by the external magnetic field, and said 1st magnetic layer. The magnetic storage film equipped with the 2nd magnetic layer which changes the sense of magnetization by said external magnetic field, and the nonmagnetic conductive layer which it is arranged [conductive layer] between said 1st and 2nd magnetic layers, and carries out antiferromagnetism association of said 1st and 2nd magnetic layers, The tunnel junction component which equips said magnetic storage film with the 2nd ferromagnetism magnetization fixing film by which opposite arrangement was carried out at said 2nd magnetic layer through the 2nd tunnel insulator layer by which contiguity arrangement was carried out, and said 2nd tunnel insulator layer is provided. The magnetic memory apparatus characterized by detecting the current difference or load electrical-potential-difference difference of the 1st tunnel current which flows between said magnetic storage film and said 1st ferromagnetism magnetization fixing film, and the 2nd tunnel current which flows between

said magnetic storage film and said 2nd ferromagnetism magnetization fixing film by the differential method.
[Claim 4] The magnetic memory apparatus according to claim 3 characterized by having the 1st wiring which carries out electrical connection to said magnetic storage film, the 2nd wiring which carries out electrical connection to said 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to said 2nd ferromagnetism magnetization fixing film.
[Claim 5] Said 1st ferromagnetism magnetization fixing film, said 1st tunnel junction film, said 1st magnetic layer, said nonmagnetic conductive layer, said 2nd magnetic layer, said 2nd tunnel junction film, and said 2nd ferromagnetism magnetization fixing film are a magnetic memory apparatus given in either claim 1 characterized by carrying out laminating formation, and claim 3.
[Claim 6] Said magnetic storage film is a magnetic memory apparatus given in either of claims 1 and 4 characterized by connecting with one side of the source drain electrode of a transistor through said 1st wiring.
[Claim 7] Said 2nd and 3rd wiring is magnetic memory apparatus given in either of claims 1 and 4 characterized by connecting with a sense amplifier.
[Claim 8] the memory cell which consists of said tunnel junction component and said transistor -- a line writing direction and the direction of a train -- the shape of an array -- **** -- the magnetic memory apparatus according to claim 6 characterized by things.
[Claim 9] The magnetic memory apparatus according to claim 8 characterized by having two or more [of said 2nd and 3rd wiring extended to said 1st wiring extended in said direction of a train, and said line writing direction].
[Claim 10] The gate electrode of two or more of said cel transistors located in a line in said direction of a train is a magnetic memory apparatus according to claim 9 characterized by making common connection at wiring of one.
[Claim 11] It is the magnetic memory apparatus according to claim 9 which common connection of the 1st ferromagnetic magnetization fixing film of two or more of said tunnel junction components on a par with said line writing direction is made at said 2nd wiring, and is characterized by making common connection of the 2nd ferromagnetic magnetization fixing film at said 3rd wiring.
[Claim 12] Said 2nd and 3rd wiring is magnetic memory apparatus according to claim 5 characterized by having-two wiring for magnetic writing which said whose tunnel junction component is pinched from the upper and lower sides, and crosses mutually.
[Claim 13] It is the magnetic memory apparatus according to claim 7 characterized by having a switch between any 1 and the sense amplifiers of said 2nd and 3rd wiring, and equipping wiring connected with said switch with wiring for magnetic writing which intersects another wiring.
[Claim 14] A magnetic memory apparatus given in either of claims 1 and 4 characterized by having the electrode layer which is formed on the same layer as the film which is separated from a substrate principal plane among said 1st ferromagnetism magnetization fixing film and said 2nd ferromagnetism magnetization fixing film, and was formed, and connects said magnetic storage film with said 1st wiring electrically.
[Claim 15] Said magnetic storage film is a magnetic memory apparatus given in either claim 1 characterized by connecting with diode through said 1st wiring, and 4 publications.
[Claim 16] the metal with which said nonmagnetic conductive layer is chosen from Cu, Ru, Cr, Re, and Ir, or Cu, Ru, Cr, Re and Ir -- more than 50atom% -- a magnetic memory apparatus given in either of claims 1 and 3 characterized by consisting of an included alloy.
[Claim 17] Claim 1 characterized by the thickness of said 1st and 2nd ferromagnetic layers differing mutually, and a magnetic memory apparatus according to claim 3.
[Claim 18] Said 1st and 2nd ferromagnetic layers are claim 1 characterized by consisting of a magnetic material with which the magnetic moments differ mutually, and a magnetic memory apparatus according to claim 3.
[Claim 19] The 1st ferromagnetism magnetization fixing film with which the magnetization direction was fixed, the 1st tunnel insulator layer by which contiguity arrangement was carried out with said 1st

ferromagnetism magnetization fixing film, And it has the 1st magnetic film which opposite arrangement is carried out with said 1st ferromagnetism magnetization fixing film through said 1st tunnel insulator layer, and changes the sense of magnetization by the external magnetic field. The sense of electric resistance of magnetization of said 1st magnetic film is low in the sense and abbreviation parallel condition of said fixed magnetization. The sense of magnetization of said 1st ferromagnetic in the state of sense substantially antiparallel [of said fixed magnetization] The 1st tunnel junction section with high electric resistance, The 2nd ferromagnetism magnetization fixing film with which the magnetization direction was fixed, the 2nd tunnel insulator layer by which contiguity arrangement was carried out with said 2nd ferromagnetism magnetization fixing film, And opposite arrangement is carried out with said 2nd ferromagnetism magnetization fixing **** through said 2nd tunnel insulator layer. Have the 2nd magnetic film which changes the sense of magnetization by the external magnetic field, and the sense of electric resistance of magnetization of said 2nd magnetic film is low in the sense and abbreviation parallel condition of said fixed magnetization. The sense of magnetization of said 2nd magnetic film in the state of sense substantially antiparallel [of said fixed magnetization] The 2nd tunnel junction section with high electric resistance, The nonmagnetic electric conduction film which connects electrically said the 1st and said 2nd magnetic film, and the cel switch which carries out electrical connection to said nonmagnetic electric conduction film, The magnetic memory apparatus characterized by having the 2nd wiring which carries out electrical connection to said 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to said 2nd ferromagnetism magnetization fixing film.

[Claim 20] Said 1st and 2nd tunnel junction section and the magnetic memory apparatus according to claim 19 characterized by having the memory cell which consists of said cel switches in the shape of an array in a line writing direction and the direction of a train.

[Claim 21] Said 1st tunnel junction section and said 2nd tunnel junction section are a magnetic memory apparatus according to claim 19 characterized by for the resistance which is always one side being high resistance, and resistance of another side being low resistance.

[Claim 22] It is the magnetic memory apparatus according to claim 19 which laminating formation of said 1st tunnel junction and said 2nd tunnel junction is carried out so that said nonmagnetic electric conduction film may be arranged between said 1st and 2nd magnetic films, and is characterized by said nonmagnetic electric conduction film carrying out antiferromagnetism association of said 1st and 2nd magnetic films.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is concerned with the information storage device which used the magnetic film, and relates to the magnetic memory apparatus using especially a ferromagnetic tunnel junction.
[0002]
[Description of the Prior Art] On the other hand, in the cascade screen with two magnetic layers by which laminating arrangement was carried out on both sides of the non-magnetic layer, it was discovered in recent years that a kind of a magneto-resistive effect (MagnetoResistance) and the so-called huge magnetic-reluctance (GiantMR) effectiveness are acquired. This carries out the laminating of a magnetic layer and the non-magnetic layer by turns with the period of several nm, and it is reported that the magnetic moment of the magnetic layer which faces through a non-magnetic layer is realizable with the cascade screen magnetically combined in the anti-parallel condition and the so-called artificial grid film. For example, artificial grid film of Fe/Cr (Phys.Rev.Lett.61, 2472 (1988) reference) It is the artificial grid film (J. Magn.Magn.Mater .. 94, L1 (1991), Phys.Rev.Lett.66, 2152 (1991) reference) of Co/Cu etc.
[0003] Moreover, it sets on the metal sandwiches film which consists of the ferromagnetic layer / a non-magnetic layer / a ferromagnetic layer which carried out the laminating of the ferromagnetic layer through the non-magnetic metal layer. By thickening thickness of a non-magnetic metal layer at extent whose switched connection between ferromagnetic layers is lost, and arranging and carrying out switched connection of the antiferromagnetism film, such as FeMn, in contact with one ferromagnetic layer The magnetic moment of the ferromagnetic layer is fixed and the so-called spin bulb film which enabled it to switch only magnetization (spin) of the ferromagnetic layer of another side easily in an external magnetic field is known (refer to [5,206,590th] United States patent). In this case, since the switched connection between two ferromagnetic layers is weak and spin can be reversed in a small magnetic field, compared with the artificial grid film, a magneto-resistive effect component with high sensibility can be offered, and current utilization is carried out as the reproducing head for high density magnetic recording.
[0004] Although the above is a magneto-resistive effect at the time of passing the current within a field in parallel with the film surface of a cascade screen, if the so-called perpendicular magneto-resistive effect which passes a current perpendicularly is used for a film surface, it is known that a still bigger magneto-resistive effect will be acquired (Phys.Rev.Lett.66, 3060 (1991) reference).
[0005] Furthermore, in three layer membranes which consist of a magnetic layer / an insulating layer / a magnetic layer, the huge magnetic-reluctance (TMR) effectiveness by the ferromagnetic tunnel junction using the magnitude of the tunnel current of a film surface perpendicular direction being mutually different is also known by making the spin of two ferromagnetic layers parallel or anti-parallel mutually by the external magnetic field (J. Magn.Magn.Mater.139 and L231 (1995)).
[0006] Moreover, the ferromagnetic duplex tunnel junction component which consists of three magnetic

layers of a magnetic layer / insulating layer / magnetic layer / insulating layer / magnetic layer and two insulating layers equipped with two insulating layers is also exhibited (JP,8-69581,A). Furthermore, the ferromagnetic duplex tunnel junction component which made the ferromagnetic of the center across which the insulating layer of both sides faced the shape of a particle is indicated by JP,10-308313,A. These ferromagnetic duplex tunnel junction components have the features that the fall of the TMR effectiveness by bias voltage is small.

[0007] On the other hand, using for a non-volatile MAG memory apparatus (MRAM: Magnetoresistive random access memory) is also studied recently instead of using a giant magneto-resistance component for field sensors, such as the magnetic head, (85 J. Appl.Phys. 85, 5822 (1999), J.Appl.Phys. 5828 . (1999)). In this case, the pseudo-spin bulb component and the ferromagnetic tunnel effect component whose non-magnetic metal layer was pinched in two ferromagnetic layers from which coercive force differs are examined. When using for MRAM, "1" and "0" are made to memorize by controlling mutually magnetization of two magnetic layers which arrange these components in the shape of a matrix so that it may spread in a line writing direction and the direction of a train, pass a current to wiring which prepared independently, impress a field, and constitute each component to parallel and anti-parallel. Read-out is performed using GMR or the TMR effectiveness.

[0008] Since the pseudo-spin bulb component using the GMR effectiveness can pass a current for a component, connects two or more components with series and tends to large-capacity-ize them, it is suitable for MRAM. However, since it is necessary to reverse the spin of the small magnetic layer of coercive force also in case it records, and it reads, that it is necessary to reverse the spin of the large magnetic layer of coercive force and, and, it is necessary to pass a comparatively big current also in any of writing and read-out of information, and is not a low-power mold. Moreover, since resistance is small, output voltage is small, therefore it is difficult to read at high speed.

[0009] There are the features, like on the other hand, there are not bigger output voltage's being obtained, since MRAM using the TMR effectiveness component has MR rate of change as large as 20% or more in a room temperature and resistance is strong, and the need of carrying out spin reversal at the time of read-out, and read so much, and a current is small and ends, and it is expected as nonvolatile memory of the possible low-power mold of high-speed writing and read-out. However, the TMR effectiveness will be reduced by half if the bias voltage whose TMR component TMR falls greatly with bias voltage and is usually 300 - 400 mV extent is impressed. Although the method which passes a fixed read-out current and obtains a signal level was taken since MRAM was a current drive mold, it was the problem for high-speed read-out that a fall it is not avoided for a sense current that the bias of 300 - 400 mV extent will be at least 10micro impressed if the magnitude of the bond resistance of a tunnel magneto-resistive effect component is considered, since it is [about A] required, but according to the bias voltage of the TMR effectiveness was big. this invention persons are doing header patent application of the effectiveness of using the multiplex tunnel junction more than a duplex which was already described to this problem. However, even if it uses a multiplex tunnel junction, it cannot be said that the conventional MRAM architecture is still enough as output voltage.

[0010] The conventional MRAM architecture carries out parallel connection of the bit line 2 to the ferromagnetic tunnel junction (hereafter referred to as MTJ) components 1a and 1b through the transistors 4a and 4b for component selection by which ON/OFF control is carried out with word lines 3a and 3b, as shown in the circuit diagram of drawing 8 . Series connection of each MTJ components 1a and 1b and the transistors 4a and 4b for component selection is carried out. The bit line with which the transistor for selection of a bit line 2 and 6 are connected to a sense amplifier, and 7 is connected to a reference cel for five in drawing 8 , and 8 are plate lines connected to the other end of the edge connected with the transistors 4a and 4b of the TMR components 1a and 1b.

[0011] In this circuit, since it is necessary to pass a current to the transistors 4a and 4b which connected with the MTJ components 1a and 1b at the time of read-out, if variation is in transistor characteristics, the noise resulting from it cannot be disregarded. For example, although read-out is usually performed in drawing 8 by judging "1" and "0" as compared with the electrical potential difference of the reference cel connected to a bit line 7 By Vs(ing) and beginning to read a read-out signal level, for a current, if

resistance of MR and a transistor is written to be r and the variation is written to be beta for the resistance rate of change of R and its TMR, resistance of Is and the MTJ components 1a and 1b Vs =TMRxRxIs/2-betarIs (1)
It becomes.
[0012] That is, only the one half of the resistance change accompanying the TMR effectiveness will be able to be used, but moreover the variation in transistor characteristics will become a noise, and a signal level will reduce a signal level. For this reason, the signal-to-noise-ratio S/N ratio of such MRAM is as small as about 30dB. This is the result of the architecture which uses a reference cel bringing. For example, using the usual value beta= 0.2 over Transistors 1a and 1b when r=1kohm, Is=10microA, R=40kohm, and TMR=25%, they are Vs=48mV and betarIs=2mV. Therefore, a S/N ratio is set to 20log (48/2) =27.6dB.
[0013] In order to aim at the improvement of such a S/N ratio, two transistors and two MTJ components are used as 1 bit, and it writes in two MTJ components so that magnetization may always become anti-parallel mutually, and the architecture of reading by the differential detecting method is proposed (the international congress announcement on ISSCC, February, 2000).
[0014] On the other hand, if a transistor is used for component selection, since the size of a transistor is larger than a MTJ component, bit size will become large, and large capacity-ization of MRAM has the fault of being prescribed by the transistor. In order to cancel this, diode is used instead of a transistor, and the structure which carried out series connection of the MTJ component to this is proposed. (Proc.of Int'l.Non.Volatile Memory Technology Conf.P47 (1998), IEEE Trans.Mag.35, and 2832 (1999)) .
[0015]
[Problem(s) to be Solved by the Invention] Writing in two MTJ components so that magnetization may always become anti-parallel mutually using two above-mentioned transistors and two MTJ components as 1 bit, by the method read by the differential detecting method, the reference cel for carrying out differential detection becomes unnecessary, and a signal level serves as Vs =TMRxRxIs and becomes twice [more than] (1) type large. However, it is thought that the cell size of 1 bit is large since 1 bit is constituted from two elements, and it is difficult to realize large capacity MRAM.
[0016] Moreover, diode is used instead of a transistor, with the structure which carried out series connection of the MTJ component to this, a reference cel is needed like **** and read-out of information has the problem which a S/N ratio says is bad.
[0017] In view of such a situation, the technical problem of this invention has a big signal level and big S/N, and is in offer of the magnetic new memory apparatus which contributes to large capacity-ization.
[0018]
[Means for Solving the Problem] The 1st ferromagnetism magnetization fixing film with which, as for the first invention, the magnetization direction was fixed in view of the above-mentioned technical problem, The 1st magnetic layer which opposite arrangement is carried out with the 1st ferromagnetism magnetization fixing film through the 1st tunnel insulator layer by which contiguity arrangement was carried out with the 1st ferromagnetism magnetization fixing film, and the 1st tunnel insulator layer, and changes the sense of magnetization by the external magnetic field, The magnetic storage film equipped with the nonmagnetic conductive layer to which it is arranged between the 2nd magnetic layer which carries out antiferromagnetism association with the 1st a little more than magnetic layer, and changes the sense of magnetization by the external magnetic field, the 1st, and the 2nd a little more than magnetic layer, and antiferromagnetism magnetic coupling of the 1st and 2nd magnetic layers is carried out, The tunnel junction component which equips the magnetic storage film with the 2nd ferromagnetism magnetization fixing film by which opposite arrangement was carried out at the 2nd magnetic layer through the 2nd tunnel insulator layer by which contiguity arrangement was carried out, and the 2nd tunnel insulator layer, The magnetic memory apparatus characterized by having the 1st wiring which carries out electrical connection to the magnetic storage film, the 2nd wiring which carries out electrical connection to the 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to the 2nd ferromagnetism magnetization fixing film is offered.
[0019] The 1st ferromagnetism magnetization fixing film with which, as for the second invention, the

magnetization direction was fixed in view of the above-mentioned technical problem, Opposite arrangement is carried out with the 1st ferromagnetism magnetization fixing film through the 1st tunnel insulator layer by which contiguity arrangement was carried out with the 1st magnetic film, and the 1st tunnel insulator layer. The 1st magnetic layer which changes the sense of magnetization by the external magnetic field, the 2nd magnetic layer which carries out antiferromagnetism association with the 1st magnetic layer, and changes the sense of magnetization by said external magnetic field, And the magnetic storage film equipped with the nonmagnetic conductive layer which it is arranged [conductive layer] between the 1st and 2nd magnetic layers, and carries out antiferromagnetism association of the 1st and 2nd magnetic layers, The 2nd tunnel insulator layer by which contiguity arrangement was carried out at the magnetic storage film, and the 2nd ferromagnetism magnetization fixing film by which opposite arrangement was carried out through the 2nd tunnel insulator layer at the 2nd magnetic layer, The magnetic memory apparatus characterized by detecting the current value or load electrical potential difference of the 1st tunnel current which flows from the magnetic storage film to the 1st ferromagnetism magnetization fixing film, and the 2nd tunnel current which flows from the magnetic storage film to the 2nd ferromagnetism magnetization fixing film by the differential method is offered.

[0020] Moreover, the 1st ferromagnetism magnetization fixing film with which, as for the third invention, the magnetization direction was fixed in view of the above-mentioned technical problem, It has the 1st tunnel insulator layer by which contiguity arrangement was carried out with the 1st ferromagnetism magnetization fixing film, and the 1st magnetic film which the 1st ferromagnetism magnetization fixing film opposite arrangement is carried out through the 1st tunnel insulator layer, and changes the sense of magnetization by the external magnetic field. Electric resistance is low in the sense of fixed magnetization of the sense of magnetization of the 1st magnetic film, and the abbreviation parallel condition. The sense of magnetization of the 1st magnetic film in the state of sense substantially antiparallel [of fixed magnetization] The 1st tunnel junction section with high electric resistance, The 2nd tunnel insulator layer by which contiguity arrangement was carried out with the 2nd ferromagnetism magnetization fixing film and the 2nd ferromagnetism magnetization fixing film with which the magnetization direction was fixed, And opposite arrangement is carried out with the 2nd ferromagnetism magnetization fixing **** through said 2nd tunnel insulator layer. Have the 2nd magnetic film which changes the sense of magnetization by the external magnetic field, and electric resistance is low in the sense of fixed magnetization of the sense of magnetization of the 2nd magnetic film, and the abbreviation parallel condition. The sense of magnetization of the 2nd magnetic film in the state of sense substantially antiparallel [of fixed magnetization] The 2nd tunnel junction section with high electric resistance, The magnetic memory apparatus characterized by having the nonmagnetic electric conduction film which connects electrically the 1st and said 2nd magnetic film, the cel switch which carries out electrical connection to the nonmagnetic electric conduction film, the 2nd wiring which carries out electrical connection to the 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to the 2nd ferromagnetism magnetization fixing film is offered.

[0021] In the magnetic memory apparatus of the first invention, it is desirable to have a means by which a differential method detects the current difference or load electrical-potential-difference difference of the 1st tunnel current which flows from the magnetic storage film to the 1st ferromagnetism magnetization fixing film, and the 2nd tunnel current which flows from the magnetic storage film to the 2nd ferromagnetism magnetization fixing film.

[0022] In the magnetic memory apparatus of the second invention, it is desirable to have the 1st wiring which carries out electrical connection to the magnetic storage film, the 2nd wiring which carries out electrical connection to the 1st ferromagnetism magnetization fixing film, and the 3rd wiring which carries out electrical connection to the 2nd ferromagnetism magnetization fixing film.

[0023] As for the magnetic memory apparatus of the second invention of the first ****, it is desirable to have the following gestalt.

1) The 1st ferromagnetism magnetization fixing film, the 1st tunnel junction film, the 1st magnetic layer, a nonmagnetic conductive layer, the 2nd magnetic layer Laminating formation of the 2nd tunnel junction film and the 2nd ferromagnetism magnetization fixing film is carried out.

2) Connect the magnetic storage film to one side of the source drain electrode of a cel transistor through the 1st wiring. It is carried out.
3) The 2nd and 3rd wiring is connected to the same sense amplifier by each end.
4) It is ARE to a line writing direction and the direction of a train about the memory cell which consists of a tunnel junction component and a cel transistor. It is **** to the shape of I.
5) It has the 2nd and 3rd-two or more wiring extended to the 1st wiring extended in the direction of a train, and a line writing direction.
6) The gate electrode of two or more cel transistors located in a line in the direction of a train in the shape of an array is common connection to wiring of one. It is carried out.
7) Common connection of two or more tunnel junction components on a par with a line writing direction in the shape of an array is made at the 2nd and 3rd wiring. ******.
8) Pinch the tunnel junction component of wiring [2nd and 3rd] from the upper and lower sides, and it intersects the 2nd and 3rd wiring. It has-two wiring for magnetic writing.
9) It has a switch between either of the 2nd and 3rd wiring, and a sense amplifier, and is the 2nd and the 3rd. It has-one wiring for magnetic writing which intersects wiring.
10) Separate from a substrate principal plane most among the 1st ferromagnetism magnetization fixing film and the 2nd ferromagnetism magnetization fixing film, and it is a form. It is formed on the same layer as the accomplished ferromagnetic magnetization fixing film, and is about the 1st wiring and the magnetic storage film. It has the electrode layer to connect.
11) The magnetic storage film is connected to diode through the 1st wiring.
12) the metal with which a nonmagnetic conductive layer is chosen from Cu, Ru, Cr, Re, and Ir, or Cu Ru, Cr, Re, and Ir -- more than 50atom% -- it consists of an included alloy.
13) The thickness of the 1st and 2nd magnetic layers differs mutually.
14) The 1st and 2nd magnetic layers consist of a magnetic material with which the magnetic moments differ mutually.
[0024] In the magnetic memory apparatus of the third invention, it has the 1st and 2nd tunnel junction section and the memory cell which consists of cel switches in the shape of an array. Moreover, the mutual magnetization of the 1st and 2nd tunnel junction section is always parallel to anti-parallel (mutual resistance always becomes the combination of high resistance and low resistance). Moreover, laminating formation of the 1st tunnel junction and the 2nd tunnel junction is carried out so that the nonmagnetic electric conduction film may be arranged between the 1st and 2nd magnetic films. Moreover, a cel switch can consist of a transistor or diode. Moreover, 15 Laminating formation of the 1st ferromagnetism magnetization fixing film, the 1st tunnel junction film, the 1st magnetic layer, a nonmagnetic conductive layer, the 2nd magnetic layer, the 2nd tunnel junction film, and the 2nd ferromagnetism magnetization fixing film is carried out.
16) The 2nd and 3rd wiring is connected to the same sense amplifier by each end.
17) It is **** to the shape of an array in a line writing direction and the direction of a train about the memory cell which consists of a tunnel junction component and a cel switch.
18) It has the 2nd and 3rd-two or more wiring extended to the 1st wiring extended in the direction of a train, and a line writing direction.
19) Common connection of the gate electrode of two or more cel transistors located in a line in the direction of a train in the shape of an array is made at wiring of one.
20) Common connection of two or more tunnel junction components on a par with a line writing direction in the shape of an array is made at the 2nd and 3rd wiring.
21) The tunnel junction component of wiring [2nd and 3rd] is pinched from the upper and lower sides, and it is equipped with-two wiring for magnetic writing which intersects the 2nd and 3rd wiring.
22) It has a switch between either of the 2nd and 3rd wiring, and a sense amplifier, and has-one wiring for magnetic writing which intersects the 2nd and 3rd wiring.
23) It is formed on the same layer as the ferromagnetic magnetization fixing film which is most separated from a substrate principal plane among the 1st ferromagnetism magnetization fixing film and the 2nd ferromagnetism magnetization fixing film, and was formed, and has the electrode layer which

connects the magnetic storage film with the 1st wiring electrically.
24) the metal with which a nonmagnetic conductive layer is chosen from Cu, Ru, Cr, Re, and Ir, or Cu, Ru, Cr, Re and Ir -- more than 50atom% -- it consists of an included alloy.
[0025]
[Embodiment of the Invention] (Gestalt of the 1st operation) The 1st operation gestalt about the circuitry of the magnetic memory apparatus of this invention is hereafter explained using the circuit diagram of drawing 1 .
[0026] The magnetic memory apparatus of this invention equips each of two or more memory cells to constitute with two or more tunnel junctions. Although the 1st operation gestalt explains using the double tunnel junction component 11 equipped with two tunnel junctions, the gestalt which extended this to the multiplex tunnel junction is also included in this invention.
[0027] The configuration of the double tunnel junction components 11a and 11b shown in drawing 1 is explained using the component of 11a. Component 11a is equipped with tunnel junction 11a-1 which consists of the 1st ferromagnetic magnetization fixing film / the 1st tunnel insulator layer / magnetic layer, and tunnel junction 11a-2 which consist of the 2nd ferromagnetic layer / the 2nd tunnel insulator layer / the 2nd ferromagnetic magnetization fixing film. [1st] If the laminating of these is carried out one by one, it will become the order of a laminating like the 1st ferromagnetic magnetization fixing film / the 1st tunnel insulator layer / the 1st magnetic layer / nonmagnetic conductive layer / the 2nd magnetic layer / the 2nd tunnel insulator layer / 2nd ferromagnetic magnetization fixing film.
[0028] The 1st and 2nd ferromagnetism magnetization fixing film is a ferromagnetic to which magnetization was fixed, and the magnetization does not change in a signal field. The 1st and 2nd magnetic layers always carry out antiferromagnetism association of the magnetization of the 1st and 2nd magnetic layers with the mutual nonmagnetic conductive layer inserted in between. Although the 1st and 2nd magnetic layers and a nonmagnetic conductive layer are collectively used as the magnetization storage film, it is the 1st and 2nd magnetic layers that the sense of magnetization changes by impression of a signal field.
[0029] Differential detection of the storage information on these tunnel junction components 11a and 11b is explained using tunnel junction component 11a of drawing 1 . informational storage -- always -- each -- it carries out so that one side of tunnel junction 11a-1 and 11a-2 may serve as the low resistance RP and another side may serve as the high resistance RAP. Here, magnetization of the magnetic layer which constitutes the tunnel junction with the same low resistance RP, and the ferromagnetic magnetization fixing film is resistance in the parallel condition mutually, and the magnetization of a ferromagnetic layer and the ferromagnetic fixing film of the high resistance RAP is resistance in the condition of anti-parallel mutually.
[0030] If the tunnel current of hard flow is mutually passed to this tunnel junction 11a-1 and 11a-2, the difference of the flowing tunnel current value or a load electrical potential difference can carry out differential detection of each junction as the sum. The tunnel current of hard flow is a current which flows from the 1st magnetic layer to the 1st magnetic magnetization fixing film through the 1st tunnel insulator layer, and flows from the 2nd magnetic layer to the 2nd magnetic magnetization fixing film through the 2nd tunnel insulator layer in tunnel junction 11a-2 in tunnel junction 11a-1 mutually. Or the current which flows from the 1st magnetic magnetization fixing film to the 1st magnetic layer to the 2nd magnetic layer again through the 2nd magnetic magnetization fixing film to 2nd tunnel insulator layer through the 1st tunnel insulator layer is sufficient.
[0031] Since the 1st ferromagnetic magnetization fixing film is connected to a bit line 13, the 2nd ferromagnetic magnetization fixing film is connected to a bit line 12 and this double tunnel junction component 11a is connected to the common sense amplifier 17, differential detection of a current difference or a load electrical-potential-difference difference is attained by passing the current of hard flow mutually.
[0032] Electrical connection of the storage film is carried out to the source drain of transistor 14a of drawing 1 . This is made with the 1st magnetic layer which constitutes the storage film, nonmagnetic conductive layers, all the 2nd magnetic layer, and a certain configuration by which is, and crawls and

electrical connection is carried out to a source drain through a conductive layer in whether it is a gap.
[0033] Parallel connection of other double tunnel junction components with the same configuration as double tunnel junction component 11a, for example, the double tunnel junction component 11of drawing 1 b, is carried out to bit lines 12 and 13 in the same format as component 11a. Moreover, connection between the storage film of the double tunnel junction component 11b and cel transistor 14b as well as it of double tunnel junction component 11a is made.
[0034] Two or more tunnel junction components connected to the same bit lines 12 and 13 can prepare more than one, and are arranged in the shape of an array in the direction in which the bit lines 12 and 13 of drawing 1 are extended. Moreover, as for the cel transistors 14a and 14b of the memory cell connected to the same bit line of drawing 1 , common connection of the many items of a source drain is made at the source drain of the pass transistor 15. The gate of each cel transistor is connected to the corresponding word lines 16a and 16b. Under the present circumstances, although not illustrated, common connection of the gate electrode of the cel transistor of the memory cell arranged in the shape of an array in the die-length direction of a word line can be made at the same word line.
[0035] While it becomes unnecessary to be able to constitute one memory cell, to be able to realize a differential method, and to use a reference cel by one transistor and the double tunnel junction component with the 1st operation gestalt, it can contribute to contraction of bit size greatly, and large-capacity-izing of a memory apparatus is possible. Moreover, since the problem of the variation in a cel transistor can be reduced, a noise can be reduced sharply, and compared with MRAM of the result former, a S/N ratio big 10 or more times is obtained. Moreover, in order to use the multiplex tunnel junction more than a duplex, the bias dependency of TMR is also small. Moreover, by the small current, since the storage film is equipped with the 1st and 2nd ferromagnetic layers combined in antiferromagnetism, even if an anti-field is small and a memory cell becomes small, since efficient writing is possible, the small mass nonvolatile memory of power consumption can be offered.
(Gestalt of the 2nd operation) Writing/read-out of magnetic information are explained to be the structures of the memory apparatus which constitutes the circuit explained in the 1st operation gestalt from the 2nd operation gestalt using the sectional view of drawing 2 . In addition, the same sign is given to the configuration same among drawing 2 as drawing 1 , and the detailed explanation is omitted.
[0036] In the double tunnel junction component 11 of this operation gestalt, laminating formation of the 1st ferromagnetic magnetization fixing film 21/the 1st magnetic layer [2nd] 25 of 24/of the 23/nonmagnetic conductive layers of 1st magnetic layer of 22/of tunnel insulator layers/the 2nd tunnel insulator layer 26/the 2nd ferromagnetic magnetization fixing film 27 is carried out one by one, and the 2nd magnetic layer of 24/of the 23/nonmagnetic conductive layers of 1st magnetic layer constitutes the storage film 28. The 1st tunnel junction is constituted by the 1st ferromagnetic magnetization fixing film 21/the 1st magnetic layer [1st] 23 of 22/of tunnel insulator layers, and, as for this component 11, the 2nd tunnel junction is constituted by the 2nd magnetic layer 25/the 2nd tunnel insulator layer 26/the 2nd ferromagnetic magnetization fixing film 27. Although the storage film 28 is a three-tiered structure, considering as multilayers further is also possible. In addition, the part which attached hatching in drawing 2 thru/or drawing 4 , drawing 6 , and drawing 7 (slash) is an interlayer insulation film.
[0037] Magnetic coupling of the 1st and 2nd magnetic layers 23 and 25 of each other which constitute the storage film 28 is carried out in antiferromagnetism. That is, magnetization of the 1st and 2nd magnetic layers 23 and 25 is held mutually at the reverse sense, and mutual magnetization is maintained by the reverse sense even after being reversed with an external magnetic field. Such antiferromagnetism-magnetic coupling is realizable by inserting the thin nonmagnetic conductive layer 24 in between the 1st and 2nd magnetic layers 23 and 25.
[0038] although the ingredient of the nonmagnetic conductive layer 24 which urges switched connection to the 1st and the 2nd a little more than magnetic layer is selectable from a well-known thing -- Cu, Ru, Cr, Re, Ir(s), and these one -- more than 50atom% -- it is desirable to use the included alloy. Since antiferromagnetism switched connection is obtained by thickness with antiferromagnetism switched connection thin strong moreover, especially Ru, Re, and Ir are desirable.
[0039] Moreover, in order to urge the flux reversal by the low current field, as for two magnetic layers

which carried out antiferromagnetism association, it is desirable for the values of magnetization to differ mutually. Therefore, it is desirable to use the magnetic layer of an ingredient which the thickness of the 1st and 2nd magnetic layers differs, or is different.

[0040] Magnetization of the 1st and 2nd ferromagnetic magnetization fixing film 21 and 27 is that magnetization of ****** which fixes in the same direction mutually, and the 1st and 2nd magnetic layers 23 and 25 which carried out antiferromagnetism association is reversed from the condition of "1" of drawing 2 to the condition of "0", as shown in drawing 2 , and a change of the storage information on this memory cell is made.

[0041] Since the sense of magnetization of the 1st ferromagnetic magnetization fixing film 21 and the 1st magnetic layer 23 is anti-parallel mutually and the condition of "1" of drawing 2 has the mutually parallel sense of magnetization of the 1st tunnel junction of the high resistance RAP, the 2nd magnetic layer 25, and the 2nd ferromagnetism magnetization fixing film 27, the 2nd tunnel junction serves as the low resistance RP. On the other hand, since the condition of "0" of drawing 2 has the mutually parallel sense of magnetization of the 1st ferromagnetic magnetization fixing film 21 and the 1st magnetic layer 23, and the sense of magnetization of the low resistance RP, the 2nd magnetic layer 25, and the 2nd ferromagnetism magnetization fixing film 27 of the 1st tunnel junction is anti-parallel mutually, resistance of the 2nd tunnel junction can be performed with the high resistance RAP.

[0042] Next, an approach to write in such storage information is explained. for making information memorize -- the word line (WL) of drawing 2 -- it carries out to 29 and 30 by **(ing) the signal current. It is long to the longitudinal direction of the space of drawing 2 , elongation and WL30 are long to the perpendicular direction of space, and WL29 is extended. Information is memorized by passing the signal current to these both by only the double tunnel junction component 11 in that intersection. As shown in drawing 2 , the storage film 28 is connected to one side of the source drain 31 of the cel transistor 14 through the contact column (wiring) which consists of a conductive ingredient, and the source drain 31 of another side of the cel transistor 14 is connected to the pass transistor 15 of drawing 1 . If the gate 32 of a cel transistor is made to turn off in case storage actuation is performed, a current will not flow to a tunnel junction. In addition, as a dotted line shows to drawing 2 , from space, the contact column which connects one side of the source drain 31 with the storage film 28 is located in this side or the back, and crosses through a bit line 13 and a word line 29, and an interlayer insulation film.

[0043] Next, the means which reads the storage information on a memory cell is explained. the current or voltage drop mutually accompanying [by making into an ON state the gate 32 of the cel transistor 14 shown in drawing 2 / a double tunnel junction] a sink and it for the tunnel current of hard flow -- a bit line (BL) -- in the cel amplifier 14 of drawing 1 , differential detection is carried out via 12 and 13. A signal level is set to deltaV (= (RAP-RP) Id) or -deltaV corresponding to above-mentioned "1" and "0", and the magnitude of TMR itself can be used as a signal. For this reason, a very big S/N ratio is obtained. In addition, 10 of drawing 2 shows semi-conductor substrates, such as silicon, and 31 shows a source drain electrode.

[0044] Moreover, the double tunnel junction which carried out the laminating to the length shown in drawing 1 can be greatly contributed to contraction of bit size. Moreover, if a soft magnetism layer is used for two magnetic layers 23 and 25 which carried out antiferromagnetism association, since coercive force will become small, even if a field required to write in magnetic information is small and component size becomes small, a storage current does not become large but is a low-power mold.

[0045] Like the 1st operation gestalt, since it is not necessary to use a reference cel and to take into consideration the variation in a transistor or a tunnel junction component, cost can be reduced remarkably further again.

[0046] In order to enlarge read-out sensibility, it is desirable to use the large ingredient of a magneto-resistive effect for the 1st and 2nd ferromagnetism magnetization fixing film or the magnetic material of the 1st and 2nd magnetic layers. Therefore, magnetic layers 23 and 25 and the ferromagnetic magnetization fixing film 21 and 27 can use half metal, such as the magnetic substance, such as Co, Fe, CoFe, CoNi, CoFeNi, and a FeNi alloy, and NiMnSb, and Co2MnGe, etc. If half metal has a large rate of spin polarization since an energy gap exists in one spin band, and this is used, a bigger magneto-

resistive effect can be acquired and the big signal output as a result will be obtained.
[0047] Moreover, it is possible to use well-known various means for a means to fix magnetization of the ferromagnetic magnetization fixing film 21 and 27. For example, a means to use the ferromagnetic high ingredient of an anti-field for the ferromagnetic magnetization fixing film 21 and 27 rather than a synthetic field required for the flux reversal of the magnetic layers 23 and 25 of the storage film 28, Moreover, a means to make the ferromagnetic magnetization fixing film 21 and 27 carry out contact arrangement of the antiferromagnetism film, and to fix magnetization of the ferromagnetic magnetization fixing film using the switched connection of the antiferromagnetism film and the ferromagnetic magnetization fixing film, There is a means to change to the antiferromagnetism film, to make carry out contact arrangement of the hard magnetic film, and to fix magnetization of the ferromagnetic magnetization fixing film 21 and 27 by the leakage field etc. As an antiferromagnetism film ingredient used for switched connection, FeMn, IrMn, PtMn, etc. can use what is used by the usual spin bulb GMR.
[0048] Moreover, as tunnel insulator layers 22 and 26, various insulating non-magnetic materials, such as aluminum 2O3, Ta2O5, silicon oxide, and MgO, can be used. The desirable range of such thickness is 30A from 5A.
[0049] furthermore, a thin film for magnetic cells which was explained above -- molecular beam epitaxy (MBE) -- it is producible using the usual thin film deposition systems, such as law, various spatters, and vacuum deposition. Moreover, structure as shown in an operation gestalt is producible using ultra-fine processing technology and a multilayer-interconnection technique.
[0050] (Gestalt of the 3rd operation) Writing/read-out of the magnetic information are explained to be other structures of the memory apparatus which constitutes the circuit explained in the 1st and 2nd operation gestalten from the 3rd operation gestalt using the informality Fig. of the cross-section structure of drawing 3 , and a circuit. The sign same about the configuration same among drawing 3 as drawing 1 and drawing 2 is attached, and the detailed explanation is omitted.
[0051] On the other hand with this operation gestalt, it is the circuit of bit lines 12 and 13 which connected the sense amplifier 17 with the bit line 13 through the transistor 33 in drawing 3 . By drawing 2 , one of two word lines 29 and 30 is omissible with this. That is, at the time of information writing, the current is made into a sink and coincidence and the transistor 33 is made the bit line 12 and the word line 34 at the OFF state. By this, the current passed to the bit line 12 does not flow a tunnel junction, but plays the role of only field generating for writing.
[0052] In addition, to two tunnel junctions of the double tunnel junction component 11, the tunnel current of hard flow can be mutually passed by making a transistor 33 into an ON state at the time of read-out, and above-mentioned differential detection is possible.
[0053] Thus, one word line can be omitted by insertion of a transistor 33, and the number of wiring layers can be reduced.
[0054] (Gestalt of the 4th operation) Writing/read-out of the magnetic information are explained to be other structures of the memory apparatus which constitutes the circuit explained in the 1st operation gestalt from the 4th operation gestalt using the informality Fig. of the cross-section structure of drawing 4 , and a circuit. In addition, the sign same about the same configuration as drawing 1 in drawing 4 thru/or drawing 3 is attached, and the detailed explanation is omitted.
[0055] With the 4th operation gestalt, as shown in drawing 4 , connection between one side of the source drain 31 of a transistor 14 and the storage film 28 is made through a bit line 12 and the magnetic electrode 35. This establishes a hole in the 2nd tunnel insulator layer 26 and the 2nd ferromagnetic magnetization fixing film 27 which are shown in drawing 2 , and creates it by embedding an insulating material in the hole. Moreover, it may change to the ferromagnetic electrode 35, the nonmagnetic electric conduction film may be used, and deposition and processing of the nonmagnetic electric conduction film are needed apart from membrane formation of the ferromagnetic magnetization fixing film 27 in this case.
[0056] If the switch on which the current was connected to the bit line 12 and the word line 34 at the sink and the bit line 13 at the time of the writing of magnetic information is made into the OFF state by

the configuration as shown in drawing 4 , the writing of the magnetic information on the storage film 28 is possible for tunnel current to the double tunnel junction 11 by the synthetic field of two currents which do not flow but flow a bit line 12 and a word line 34.
[0057] Moreover, it becomes possible to pass a reverse current to each junction which made the transistor 33 of drawing 4 into the ON state, and it is made for a current to flow to bit lines 12 and 13, could energize for read-out of storage information to the double tunnel junction 11 by making a transistor 14 into an ON state, and was explained to it with the 1st operation gestalt.
(5th operation gestalt) Although the 1st thru/or 4th operation gestalt explained the structure and circuitry at the time of using a transistor and a tunnel junction component for a memory cell, the 5th operation gestalt explains the circuitry which used cel diode instead of the cel transistor using the circuit diagram of drawing 5 . In addition, the same sign is given to the configuration same among drawing 5 as drawing 1 thru/or drawing 4 , and the detailed explanation is omitted.
[0058] Drawing 5 is an electrical circuit at the time of replacing cel tolan Sister 14a and 14b in drawing 1 for Diodes 51a and 51b. however, since diode does not have a cel optional feature, it is made possible -- as -- drawing 5 -- a bit line (BL) -- the selection transistors 55 and 56 are formed in the end of 12 and 13. Compared with preparing a cel transistor in each memory cell, the bad influence to large-capacity-izing of a memory apparatus has few these selection transistors 55 and 56 that what is necessary is just to prepare in each one bit line.
[0059] The read-out actuation in this circuit is the same as that of what was explained in drawing 1 , except that the cel transistor 14 replaces diode 51, and detailed explanation is omitted.
[0060] Moreover, write-in actuation can be performed by passing a current to the word line for magnetic information writing which is not shown in drawing 5 , or BL 12 and 13. The current passed to BL 12 and 13 contributes only to field generating, without flowing for the tunnel junction component 11 by using diode 51. Of course, two word lines for magnetic information writing which intersect perpendicularly mutually may be used.
(Gestalt of the 6th operation) Writing and read-out of the magnetic information are explained to be the structures of the memory cell which constitutes the circuit explained in the 5th operation gestalt from the 6th operation gestalt using the informality Fig. of the cross-section structure of drawing 6 , and a circuit. In addition, about the same configuration as drawing 1 thru/or drawing 5 , the same sign is attached among drawing 6 , and the detailed explanation is omitted.
[0061] Diode 51 is formed in the upper part of the storage film 28 of the double tunnel junction component 11 in the example of drawing 6 . Diode 51 has the property that can use pn junction diode, the schottky diode using contact to a metal and a semi-conductor, the diode of other common knowledge, etc., a current flows by impression of forward voltage in junction of two layers fundamentally, and a current does not flow by impression of reverse voltage. In drawing 6 , a current is passed in WL34 for storage, and the upper part BL12, and storage information is written in them using the synthetic field. Since diode 51 exists at this time, a current does not flow for a double tunnel junction component.
[0062] Read-out of storage information can carry out differential detection by choosing the diode 51 of drawing 6 , and two BL(s) 12 and 13.
(Gestalt of the 7th operation) Writing and read-out of the magnetic information are explained to be other structures of the memory apparatus which constitutes the circuit explained in the 5th operation gestalt from the 7th operation gestalt using the informality Fig. of the cross-section structure of drawing 7 R> 7, and a circuit. In addition, about the same configuration as drawing 1 thru/or drawing 6 , the same sign is attached among drawing 7 R> 7, and the detailed explanation is omitted.
[0063] The cross-section structure which formed diode 51 in the lower part of the double tunnel junction component 11 is shown in drawing 7 . This structure performs the writing to the storage film 28 because the bottom bit line 13 passes a current to elongation and the vertical bit lines 12 and 13 for a long time to the space perpendicular direction of drawing 7 and generates a synthetic field. Since there is diode 51 too at this time, a current does not flow for the double tunnel junction component 11. Read-out can be performed by choosing WL53 extended to a space perpendicular direction by drawing 7 linked to diode,

and BL 12 and 13.
[0064] If the diode 51 explained with the 5th thru/or 7th operation gestalt is used, it reads by adjusting the resistance and a current can be adjusted. For example, it will read, if resistance of diode is enlarged, and a current becomes small, bias voltage becomes small as a result, and the big advantage that the fall of the TMR effectiveness can be controlled is brought about. In addition, the same of adjustment of such bias voltage is said of the case of the operation gestalt of the 1st which used the transistor as a switching device thru/or 4.
[0065] Although each class used for the tunnel junction component in a memory cell the double tunnel junction component by which laminating formation was carried out to the perpendicular direction of a substrate side with the 2nd [which was explained above] thru/or 4th, 6th, and 7th operation gestalt, the tunnel junction component of this invention is not restricted to this, but can be changed variously. That is, it is applicable also to the multiplex tunnel component more than a duplex. Moreover, modification of structure is possible in the range which laminating formation does not necessarily have to be carried out and does not deviate from the meaning of this invention.
[0066] Moreover, as the third invention was described, the magnetic memory apparatus of the method with which the tunnel junction of the low resistance RP and another side carries out differential detection of the current difference or load electrical-potential-difference difference of the current which constitutes so that the relation of the high resistance RAP may be maintained, and branches in a nonmagnetic conductive layer, and which flows the 1st tunnel junction, and the current which flows the 2nd tunnel junction also has the tunnel junction which is always one side within the limits of this invention using two 1-fold tunnel junctions.
[0067] Since one transistor and two tunnel junction components which connect a memory cell with a nonmagnetic conductive layer can constitute from the magnetic memory apparatus of the third invention, a transistor count can be reduced and contraction of the problem of dispersion in a switch (a transistor or diode) and the area of one cel can be realized. Moreover, it can have the property excellent in the S/N ratio.
[0068] As structure of realizing the magnetic memory apparatus of the third invention, the 1st tunnel junction linked to a nonmagnetic conductive layer and the 2nd tunnel junction can be estranged and formed in extent whose antiferromagnetism association between magnetic layers is lost. Functionally, unlike the 1st thru/or 7th already described operation gestalt, not using antiferromagnetism association of the 1st and 2nd magnetic layers by the nonmagnetic electric conduction film, the flux reversal of these magnetic layers is controlled independently, and the tunnel junction which is always one side realizes differential detection because the tunnel junction of the low resistance RP and another side gives the relation of the high resistance RAP. Therefore, a write-in line required for the flux reversal of both the ferromagnetism layer is needed for every tunnel junction.
[0069] In addition, this invention is the range which does not deviate from the meaning expressed above, and modification and combination are variously possible for it based on the 1st thru/or 7th operation gestalt.
[0070]
[Effect of the Invention] The magnetic memory apparatus of this invention can realize a differential method using one switch (a transistor and diode) and two tunnel junctions, and can realize the outstanding S/N ratio. Moreover, it can contribute to contraction of bit size greatly, and enlargement of storage capacity is possible. Moreover, since the problem of the variation in a transistor or diode can be reduced, a noise can be reduced sharply.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The circuit diagram for explaining the 1st operation gestalt of this invention.
[Drawing 2] the cross-section structure for explaining the 2nd operation gestalt of this invention, and a part -- the informality Fig. of a circuit.
[Drawing 3] the cross-section structure for explaining the 3rd operation gestalt of this invention, and a part -- the informality Fig. of a circuit.
[Drawing 4] the cross-section structure for explaining the 4th operation gestalt of this invention, and a part -- the informality Fig. of a circuit.
[Drawing 5] The circuit diagram for explaining the 5th operation gestalt of this invention.
[Drawing 6] the cross-section structure for explaining the 6th operation gestalt of this invention, and a part -- the informality Fig. of a circuit.
[Drawing 7] the cross-section structure for explaining the 7th operation gestalt of this invention, and a part -- the informality Fig. of a circuit.
[Drawing 8] The circuit diagram of the conventional magnetic memory apparatus of this invention.
[Description of Notations]
1a, 1b, 11a-1, 11a-2, 11b-1, 11b-2 -- Tunnel junction component
2, 12, 13 -- Bit line
3, 16a, 16b -- Word line for cel selection
4a, 4b, 14a, 14b -- Cel transistor
5 15 -- Pass transistor
6.17 -- Sense amplifier
7 -- Bit line for reference cels
8 -- Plate line
10 -- Substrates, such as a semi-conductor
29, 30, 34 -- Word line for writing
31 -- Source drain electrode
32 -- Gate electrode
33, 55, 56 -- Switch transistor
51, 51a, 51b -- Diode

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2001－266567
（P2001－266567A）
(43)公開日　平成13年９月28日(2001.9.28)

(51)Int.Cl.'		識別記号	FI			テーマコード'(参考)
Ｇ１１Ｃ	11/15		Ｇ１１Ｃ	11/15		５Ｅ０４９
Ｈ０１Ｆ	10/06		Ｈ０１Ｆ	10/06		５Ｆ０８３
	10/26			10/26		
	10/32			10/32		
Ｈ０１Ｌ	27/10	４５１	Ｈ０１Ｌ	27/10	４５１	

審査請求　未請求　請求項の数22　ＯＬ　（全 12 頁）　最終頁に続く

(21)出願番号　特願2000－75168(P2000－75168)

(22)出願日　平成12年３月17日(2000.3.17)

(71)出願人　000003078
株式会社東芝
東京都港区芝浦一丁目１番１号

(72)発明者　猪俣　浩一郎
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝研究開発センター内

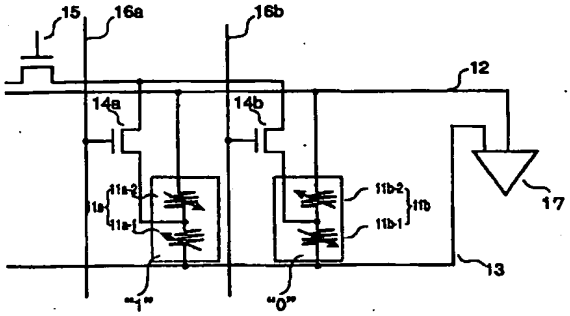
(72)発明者　中島　健太郎
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝研究開発センター内

(74)代理人　100083161
弁理士　外川　英明

最終頁に続く

(54)【発明の名称】　磁気メモリ装置

(57)【要約】
【課題】大きな信号電圧と大きなＳ/Ｎをもち、大容量化に寄与する新しい磁気メモリ装置の提供。
【解決手段】第１磁化固着膜と、第１磁化固着膜と近接配置された第１トンネル絶縁膜と、第１トンネル絶縁膜を介して第１磁化固着膜と対向配置され外部磁界により磁化の向きが変わる第１磁性層を備える第１トンネル接合１１ａ－１と、第１強磁性層と反強磁性結合して外部磁界によって磁化の向きが変わる第２磁性層、第２トンネル絶縁膜と、第２トンネル絶縁膜を介して第２磁性層に対向配置された第２磁化固着膜を備える第２トンネル接合１１ａ－２を備え、常に第１トンネル接合と第２トンネル接合の一方が低抵抗、他方が高抵抗を維持する。読み出し電流は、セルトランジスタ１６ａを介して、第１トンネル接合と第２トンネル接合に分流され、その電流差あるいは負荷電圧の差をセンスアンプ１７によって差動検出できる。



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【特許請求の範囲】

【請求項１】磁化方向が固定された第１強磁性磁化固着膜と、

前記第１強磁性磁化固着膜と近接配置された第１トンネル絶縁膜と、

前記第１トンネル絶縁膜を介して前記第１強磁性磁化固着膜と対向配置され、外部磁界により磁化の向きが変わる第１磁性層、前記第１強磁性層と反強磁性結合し、前記外部磁界により磁化の向きが変わる第２磁性層、及び前記第１及び第２強磁性層間に配置され前記第１及び第２磁性層を反強磁性結合させる非磁性導電層を備えた磁気記憶膜と、

前記磁気記憶膜に近接配置された第２トンネル絶縁膜と、

前記第２トンネル絶縁膜を介して前記第２磁性層に対向配置された第２強磁性磁化固着膜とを備えるトンネル接合素子、

前記磁気記憶膜に電気接続する第１配線、

前記第１強磁性磁化固着膜に電気接続する第２配線、及び前記第２強磁性磁化固着膜に電気接続する第３配線を備えることを特徴とする磁気メモリ装置。

【請求項２】前記磁気記憶膜と前記第１強磁性磁化固着膜との間を流れる第１トンネル電流と、前記磁気記憶膜と前記第２強磁性磁化固着膜との間を流れる第２トンネル電流との電流差、あるいは負荷電圧差を差動方式で検出することを特徴とする請求項１記載の磁気メモリ装置。

【請求項３】磁化方向が固定された第１強磁性磁化固着膜と、

前記第１磁性膜と近接配置された第１トンネル絶縁膜と、

前記第１トンネル絶縁膜を介して前記第１強磁性磁化固着膜と対向配置され、外部磁界により磁化の向きが変わる第１磁性層、前記第１磁性層と反強磁性結合し、前記外部磁界により磁化の向きが変わる第２磁性層、及び前記第１及び第２磁性層間に配置され前記第１及び第２磁性層を反強磁性結合させる非磁性導電層を備える磁気記憶膜と、

前記磁気記憶膜に近接配置された第２トンネル絶縁膜と、

前記第２トンネル絶縁膜を介して前記第２磁性層に対向配置された第２強磁性磁化固着膜とを備えるトンネル接合素子を具備し、

前記磁気記憶膜と前記第１強磁性磁化固着膜との間を流れる第１トンネル電流と、前記磁気記憶膜と前記第２強磁性磁化固着膜との間を流れる第２トンネル電流の電流差、あるいは負荷電圧差を差動方式で検出することを特徴とする磁気メモリ装置。

【請求項４】前記磁気記憶膜に電気接続する第１配線、

前記第１強磁性磁化固着膜に電気接続する第２配線、及び前記第２強磁性磁化固着膜に電気接続する第３配線を備えることを特徴とする請求項３記載の磁気メモリ装置。

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【請求項５】前記第１強磁性磁化固着膜、前記第１トンネル接合膜、前記第１磁性層、前記非磁性導電層、前記第２磁性層、前記第２トンネル接合膜、及び前記第２強磁性磁化固着膜は積層形成されていることを特徴とする請求項１及び請求項３のいずれかに記載の磁気メモリ装置。

【請求項６】前記磁気記憶膜は前記第１配線を介してトランジスタのソース・ドレイン電極の一方に接続されていることを特徴とする請求項１及び４のいずれかに記載の磁気メモリ装置。

【請求項７】前記第２及び第３配線はセンスアンプに接続されていることを特徴とする請求項１及び４のいずれかに記載の磁気メモリ装置。

【請求項８】前記トンネル接合素子及び前記トランジスタからなるメモリセルを行方向及び列方向にアレイ状に備えることを特徴とする請求項６に記載の磁気メモリ装置。

【請求項９】前記列方向に伸びる前記第１配線及び前記行方向に伸びる前記第２及び第３配線を複数本備えることを特徴とする請求項８に記載の磁気メモリ装置。

【請求項１０】前記列方向に並ぶ複数の前記セルトランジスタのゲート電極は一本の配線に共通接続されていることを特徴とする請求項９記載の磁気メモリ装置。

【請求項１１】前記行方向に並ぶ複数の前記トンネル接合素子の第１の強磁性磁化固着膜は前記第２配線に共通接続され、第２の強磁性磁化固着膜は前記第３配線に共通接続されていることを特徴とする請求項９記載の磁気メモリ装置。

【請求項１２】前記第２及び第３配線は前記トンネル接合素子を上下から挟み、互いに交差する磁気書き込み用配線を２本備えることを特徴とする請求項５記載の磁気メモリ装置。

【請求項１３】前記第２及び第３配線のいずれか一とセンスアンプとの間にスイッチを備え、前記スイッチと接続される配線は別の配線と交差する磁気書き込み用配線を備えることを特徴とする請求項７記載の磁気メモリ装置。

【請求項１４】前記第１強磁性磁化固着膜及び前記第２強磁性磁化固着膜のうち基板主面より離れて形成された膜と同一層上に形成され、前記第１配線と前記磁気記憶膜を電気的に接続する電極膜を備えることを特徴とする請求項１及び４のいずれかに記載の磁気メモリ装置。

【請求項１５】前記磁気記憶膜は前記第１配線を介してダイオードに接続されていることを特徴とする請求項１及び４記載のいずれかに記載の磁気メモリ装置。

【請求項１６】前記非磁性導電層は、Ｃｕ，Ｒｕ，Ｃｒ,Ｒｅ，Ｉｒから選ばれる金属、あるいはＣｕ，Ｒ

u，Ｃｒ，Ｒｅ，Ｉｒを５０ａｔｏｍ％以上含む合金からなることを特徴とする請求項１及び３のいずれかに記載の磁気メモリ装置。

【請求項１７】前記第１及び第２の強磁性層の厚さが互いに異なることを特徴とする請求項１及び請求項３に記載の磁気メモリ装置。

【請求項１８】前記第１及び第２の強磁性層は、互いに磁気モーメントの異なる磁性材料からなることを特徴とする請求項１及び請求項３に記載の磁気メモリ装置。

【請求項１９】磁化方向が固定された第１強磁性磁化固着膜、前記第１強磁性磁化固着膜と近接配置された第１トンネル絶縁膜、及び前記第１トンネル絶縁膜を介して前記第１強磁性磁化固着膜と対向配置され外部磁界によって磁化の向きが変わる第１磁性膜を備え、前記第１磁性膜の磁化の向きが前記固定磁化の向きと略平行状態で電気抵抗が低く、前記第１強磁性膜の磁化の向きが前記固定磁化の向き略反平行状態で電気抵抗が高い第１トンネル接合部と、

磁化方向が固定された第２強磁性磁化固着膜、前記第２強磁性磁化固着膜と近接配置された第２トンネル絶縁膜、及び前記第２トンネル絶縁膜を介して前記第２強磁性磁化固着膜膜と対向配置され、外部磁界によって磁化の向きが変わる第２磁性膜を備え、前記第２磁性膜の磁化の向きが前記固定磁化の向きと略平行状態で電気抵抗が低く、前記第２磁性膜の磁化の向きが前記固定磁化の向き略反平行状態で電気抵抗が高い第２トンネル接合部と、

前記第１及び前記第２磁性膜を電気的に接続する非磁性導電膜と、

前記非磁性導電膜に電気接続するセルスイッチと、

前記第１強磁性磁化固着膜に電気接続する第２配線と、前記第２強磁性磁化固着膜に電気接続する第３配線とを備えることを特徴とする磁気メモリ装置。

【請求項２０】前記第１及び第２トンネル接合部、及び前記セルスイッチから構成されるメモリセルを行方向及び列方向にアレイ状に備えることを特徴とする請求項１９記載の磁気メモリ装置。

【請求項２１】前記第１トンネル接合部及び前記第２トンネル接合部は、常に一方の抵抗が高抵抗であり他方の抵抗が低抵抗であることを特徴とする請求項１９記載の磁気メモリ装置。

【請求項２２】前記第１トンネル接合及び前記第２トンネル接合は、前記第１及び第２磁性膜間に前記非磁性導電膜が配置されるように積層形成され、前記非磁性導電膜は前記第１及び第２磁性膜を反強磁性結合させることを特徴とする請求項１９記載の磁気メモリ装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、磁性膜を用いた情報記憶装置に関わり、特に強磁性トンネル接合を利用した磁気メモリ装置に関する。

【０００２】

【従来の技術】一方、近年、非磁性層を挟んで積層配置された２つの磁性層を持つ積層膜において、磁気抵抗効果（ＭａｇｎｅｔｏＲｅｓｉｓｔａｎｃｅ）の一種、いわゆる巨大磁気抵抗（ＧｉａｎｔＭＲ）効果が得られることが発見された。これは、磁性層と非磁性層とを数ｎｍの周期で交互に積層し、非磁性層を介して相対する磁性層の磁気モーメントを反平行状態で磁気的に結合させた積層膜、いわゆる人工格子膜によって実現できることが報告されている。例えば、Fe/Crの人工格子膜（Phys. Rev.Lett. 61, 2472（1988）参照）や，Co/Cuの人工格子膜（J.Magn.Magn.Mater.. 94, L1（1991），Phys.Rev.Lett.66, 2152（1991）参照）等である。

【０００３】また、非磁性金属層を介して強磁性層を積層した強磁性層／非磁性層／強磁性層からなる金属サンドイッチ膜において、強磁性層間の交換結合がなくなる程度に非磁性金属層の膜厚を厚くし、かつ、一方の強磁性層に接してFeMnなどの反強磁性膜を配置して交換結合させることにより、その強磁性層の磁気モーメントを固定し、他方の強磁性層の磁化（スピン）のみを外部磁場で容易にスイッチできるようにした、いわゆるスピンバルブ膜が知られている（米国特許第5,206,590参照）。この場合、２つの強磁性層間の交換結合が弱いため小さな磁場でスピンを反転できるので人工格子膜に比べて感度の高い磁気抵抗効果素子を提供でき、高密度磁気記録用再生ヘッドとして、現在実用化されている。

【０００４】以上は積層膜の膜面に平行に、面内電流を流した場合の磁気抵抗効果であるが、膜面に垂直方向に電流を流す、いわゆる垂直磁気抵抗効果を利用すると，さらに大きな磁気抵抗効果が得られることが知られている（Phys.Rev.Lett. 66, 3060（1991）参照）。

【０００５】さらに、磁性層／絶縁層／磁性層からなる３層膜において、外部磁場によって２つの強磁性層のスピンを互いに平行あるいは反平行にすることにより膜面垂直方向のトンネル電流の大きさが互いに違うことを利用した強磁性トンネル接合による巨大磁気抵抗（TMR）効果も知られている（J. Magn. Magn. Mater. 139, L231 (1995)）。

【０００６】また、絶縁層を二つ備えた磁性層／絶縁層／磁性層／絶縁層／磁性層の三つの磁性層と二つの絶縁層からなる強磁性２重トンネル接合素子も公開されている（特開平8-69581号）。さらに、特開平10-308313号には、両側の絶縁層によって挟まれた中央の強磁性体を微粒子状にした強磁性２重トンネル接合素子が開示されている。これらの強磁性２重トンネル接合素子は、バイアス電圧によるTMR効果の低下が小さいという特長がある。

【０００７】一方、巨大磁気抵抗効果素子を磁気ヘッド等の磁界センサに使用する代わりに、不揮発性磁気メモ

リ装置(MRAM: Magnetoresistive random access memory)に利用することも最近研究されている（J.Appl.Phys. 85、5822 (1999),J. Appl. Phys.85,5828 (1999).）。この場合、保磁力の異なる二つの強磁性層で非磁性金属層を挟んだ擬スピンバルブ素子や強磁性トンネル効果素子が検討されている。MRAMへ利用する場合にはこれらの素子を行方向及び列方向に広がるようにマトリックス状に配置し、別に設けた配線に電流を流して磁界を印加して各素子を構成する二つの磁性層の磁化を互いに平行、反平行に制御することにより“１”，“０”を記憶させる。読み出しはＧＭＲやＴＭＲ効果を利用して行う。

【０００８】ＧＭＲ効果を利用した擬スピンバルブ素子は素子に電流を流すことができるため、複数の素子をシリーズにつないで大容量化し易いことから、ＭＲＡＭに適している。しかし、記録する際に、保磁力の大きい磁性層のスピンを反転する必要があること、また読み出す際にも保磁力の小さい磁性層のスピンを反転する必要があることなどから、情報の書き込み・読み出しのいずれにおいても比較的大きな電流を流す必要があり、低消費電力型ではない。また、抵抗が小さいため出力電圧が小さく、そのため高速で読み出すことが困難である。

【０００９】一方、ＴＭＲ効果素子を利用したＭＲＡＭは、室温でのＭＲ変化率が２０％以上と大きく、かつ抵抗が大きいのでより大きな出力電圧が得られること、また、読み出し時にスピン反転をする必要が無く、それだけ読み出し電流が小さくて済むことなどの特長があり、高速書き込み・読み出しの可能な低消費電力型の不揮発メモリとして期待されている。しかし、ＴＭＲ素子はバイアス電圧とともにＴＭＲが大きく低下し、通常300～400 mV程度のバイアス電圧が印加されるとＴＭＲ効果は半減する。ＭＲＡＭは電流駆動型であるので、一定の読＊み出し電流を流して信号電圧を得る方式が取られるが、高速読み出しのためにはセンス電流は少なくとも10μＡ程度必要なため、トンネル磁気抵抗効果素子の接合抵抗の大きさを考えると、300～400 mV程度のバイアスが印加されるのは避けられず、ＴＭＲ効果のバイアス電圧による低下は大きな問題であった。本発明者らはこの問題に対しては既に述べたような２重以上の多重トンネル接合を用いることの有効性を見出し特許出願している。しかし、多重トンネル接合を用いても従来のＭＲＡＭアーキテクチャでは出力電圧はまだ十分とは言えない。

$$Vs = TMR \times R \times Is/2 - \beta r Is \quad (1)$$

となる。

【００１２】すなわち、信号電圧はＴＭＲ効果に伴う抵抗変化の半分しか利用できず、しかもトランジスタ特性のバラツキがノイズとなって信号電圧を低下させてしまう。このため、このようなＭＲＡＭの信号対雑音比Ｓ/Ｎ比は30dB程度と小さい。これは参照セルを用いるアーキテクチャがもたらす結果である。例えば、トランジスタ１ａ，１ｂに対する通常の値$\beta = 0.2$を用い、ｒ=1kΩ、Ｉｓ=10μA、Ｒ=40kΩ、ＴＭＲ＝25%とするとＶｓ=48mV、$\beta r Is$ = 2mVである。従って、Ｓ/Ｎ比は20log（48/2）=27.6dBとなる。

【００１３】このようなＳ/Ｎ比の改善を図るために、二つのトランジスタと二つのＭＴＪ素子を１ビットとして用い、二つのＭＴＪ素子には常に磁化が互いに反平行になるように書き込み、差動検出法で読み出すというアーキテクチャが提案されている（ISSCC国際会議発表、2000年2月）。

【００１４】一方、素子選択用にトランジスタを用いるＭＲＡＭの大容量化はトランジスタで規定されてしまうという欠点がある。これを解消するためにトランジスタの代わりにダイオードを用い、これとＭＴＪ素子を直列接続した構造が提案されている。（Proc. of Int'l. Non. Volatile Memory Technology Conf. P47 (1998), IEEE Trans. Mag. 35, 2832 (1999)）。

【００１０】従来のＭＲＡＭアーキテクチャは図８の回路図に示すように、強磁性トンネル接合（以下、ＭＴＪとする）素子１ａ，１ｂとビット線２を、ワード線３ａ，３ｂによってＯＮ/ＯＦＦ制御される素子選択用トランジスタ４ａ，４ｂを介して並列接続する。個々のＭＴＪ素子１ａ，１ｂと素子選択用トランジスタ４ａ，４ｂは直列接続する。図８中の５はビット線２の選択用トランジスタ、６はセンスアンプ、７は参照セルに接続されるビット線、８はＴＭＲ素子１ａ，１ｂのトランジスタ４ａ，４ｂと接続される端の他端に接続されるプレート線である。

【００１１】この回路では、読み出し時にＭＴＪ素子１ａ，１ｂに接続したトランジスタ４ａ，４ｂに電流を流す必要があるため、トランジスタ特性にバラツキがあるとそれに起因するノイズが無視できない。例えば、図８において読み出しは通常、ビット線７に接続される参照セルの電圧と比較して“１”，“０”を判定して行うが、読み出し信号電圧をＶｓ、読み出し電流をＩｓ、ＭＴＪ素子１ａ，１ｂの抵抗をＲ、そのＴＭＲの抵抗変化率をＭＲ，トランジスタの抵抗をｒ，そのバラツキをβと書くと、

【００１５】

【発明が解決しようとする課題】上述の、２つのトランジスタと２つのＭＴＪ素子を１ビットとして用い、二つのＭＴＪ素子には常に磁化が互いに反平行になるように書き込み、差動検出法で読み出す方式では差動検出するための参照セルが不要となり、信号電圧はＶｓ＝ＴＭＲｘＲｘＩｓとなり、（１）式の２倍以上と大きくなる。しかし、２素子で１ビットを構成するため１ビットのセルサイズが大きく、大容量ＭＲＡＭを実現することは困難と考えられる。

【００１６】また、トランジスタの代わりにダイオードを用い、これとＭＴＪ素子を直列接続した構造では、情報の読み出しは上述と同じように参照セルが必要になり、Ｓ/Ｎ比が悪いと言う問題を抱えている。

【００１７】本発明の課題はこのような状況に鑑み、大きな信号電圧と大きなＳ/Ｎをもち、大容量化に寄与する新しい磁気メモリ装置の提供にある。

【００１８】

【問題を解決するための手段】上記課題に鑑み、第一発明は、磁化方向が固定された第１強磁性磁化固着膜と、第１強磁性磁化固着膜と近接配置された第１トンネル絶縁膜と、第１トンネル絶縁膜を介して第１強磁性磁化固着膜と対向配置され外部磁界により磁化の向きが変わる第１磁性層、第１強磁性層と反強磁性結合して外部磁界によって磁化の向きが変わる第２磁性層、及び第１及び第２強磁性層間に配置され第１及び第２磁性層を反強磁性磁気結合させる非磁性導電層を備えた磁気記憶膜と、磁気記憶膜に近接配置された第２トンネル絶縁膜と、第２トンネル絶縁膜を介して第２磁性層に対向配置された第２強磁性磁化固着膜とを備えるトンネル接合素子、磁気記憶膜に電気接続する第１配線、第１強磁性磁化固着膜に電気接続する第２配線、及び第２強磁性磁化固着膜に電気接続する第３配線を備えることを特徴とする磁気メモリ装置を提供する。

【００１９】上記課題に鑑み、第二発明は、磁化方向が固定された第１強磁性磁化固着膜と、第１磁性膜と近接配置された第１トンネル絶縁膜と、第１トンネル絶縁膜を介して第１強磁性磁化固着膜と対向配置され、外部磁界により磁化の向きが変わる第１磁性層、第１磁性層と反強磁性結合して前記外部磁界によって磁化の向きが変わる第２磁性層、及び第１及び第２磁性層間に配置され第１及び第２磁性層を反強磁性結合させる非磁性導電層を備える磁気記憶膜と、磁気記憶膜に近接配置された第２トンネル絶縁膜と、第２トンネル絶縁膜を介して第２磁性層に対向配置された第２強磁性磁化固着膜と、磁気記憶膜から第１強磁性磁化固着膜へ流れる第１トンネル電流と、磁気記憶膜から第２強磁性磁化固着膜へ流れる第２トンネル電流の電流値、あるいは負荷電圧を差動方式で検出することを特徴とする磁気メモリ装置を提供する。

【００２０】また、上記課題に鑑み、第三発明は、磁化方向が固定された第１強磁性磁化固着膜、第１強磁性磁化固着膜と近接配置された第１トンネル絶縁膜、及び第１トンネル絶縁膜を介して第１強磁性磁化固着膜対向配置され外部磁界によって磁化の向きが変わる第１磁性膜を備え、第１磁性膜の磁化の向きが固定磁化の向きと略平行状態で電気抵抗が低く、第１磁性膜の磁化の向きが固定磁化の向き略反平行状態で電気抵抗が高い第１トンネル接合部と、磁化方向が固定された第２強磁性磁化固着膜、第２強磁性磁化固着膜と近接配置された第２トンネル絶縁膜、及び前記第２トンネル絶縁膜を介して第２強磁性磁化固着膜膜と対向配置され、外部磁界によって磁化の向きが変わる第２磁性膜を備え、第２磁性膜の磁化の向きが固定磁化の向きと略平行状態で電気抵抗が低く、第２磁性膜の磁化の向きが固定磁化の向き略反平行状態で電気抵抗が高い第２トンネル接合部と、第１及び前記第２磁性膜を電気的に接続する非磁性導電膜と、非磁性導電膜に電気接続するセルスイッチと、第１強磁性磁化固着膜に電気接続する第２配線、及び第２強磁性磁化固着膜に電気接続する第３配線を備えることを特徴とする磁気メモリ装置を提供する。

【００２１】第一発明の磁気メモリ装置において、磁気記憶膜から第１強磁性磁化固着膜へ流れる第１トンネル電流と、磁気記憶膜から第２強磁性磁化固着膜へ流れる第２トンネル電流との電流差、あるいは負荷電圧差を差動方式で検出する手段を備えることが好ましい。

【００２２】第二発明の磁気メモリ装置において、磁気記憶膜に電気接続する第１配線、第１強磁性磁化固着膜に電気接続する第２配線、及び第２強磁性磁化固着膜に電気接続する第３配線を備えることが好ましい。

【００２３】第一乃び第二発明の磁気メモリ装置は次の形態を備えることが好ましい。

１）第１強磁性磁化固着膜、第１トンネル接合膜、第１磁性層、非磁性導電層、第２磁性層　　、第２トンネル接合膜、及び第２強磁性磁化固着膜は積層形成されている。

２）磁気記憶膜は第１配線を介してセルトランジスタのソース・ドレイン電極の一方に接続　　されている。

３）第２及び第３配線は夫々の一端で同一のセンスアンプに接続されている。

４）トンネル接合素子及びセルトランジスタからなるメモリセルを行方向及び列方向にアレ　　イ状に備る。

５）列方向に伸びる第１配線及び行方向に伸びる第２及び第３配線を複数本備える。

６）列方向にアレイ状に並ぶ複数のセルトランジスタのゲート電極は一本の配線に共通接続　　されている。

７）行方向にアレイ状に並ぶ複数のトンネル接合素子は、第２及び第３配線に共通接続され　　ている。

８）第２及び第３配線はトンネル接合素子を上下から挟み、第２及び第３の配線と交差する　　磁気書き込み用配線を２本備える。

９）第２及び第３配線のいずれかとセンスアンプとの間にスイッチを備え、第２及び第３の　　配線と交差する磁気書き込み用配線を１本備える。

１０）第１強磁性磁化固着膜及び第２強磁性磁化固着膜のうち、基板主面より最も離れて形　　成された強磁性磁化固着膜と同一層上に形成され、第１配線と磁気記憶膜を電気的に　　接続する電極膜を備える。

１１）磁気記憶膜は第１配線を介してダイオードに接続されている。

１２）非磁性導電層は、Ｃｕ，Ｒｕ，Ｃｒ，Ｒｅ，Ｉｒから選ばれる金属、あるいはＣｕ，Ｒｕ，Ｃｒ，Ｒｅ，Ｉｒを５０ａｔｏｍ％以上含む合金からなる。

１３）　第１及び第２の磁性層の厚さが互いに異なる。

１４）　第１及び第２の磁性層は、互いに磁気モーメントの異なる磁性材料からなる。

【００２４】第三発明の磁気メモリ装置において、第１及び第２トンネル接合部、及びセルスイッチから構成されるメモリセルをアレイ状に備える。また、第１及び第２トンネル接合部は常に互いの磁化が反平行と平行である（常に互いの抵抗は高抵抗と低抵抗の組み合わせになる）。また、第１トンネル接合及び第２トンネル接合は、第１及び第２磁性膜間に非磁性導電膜が配置されるように積層形成される。また、セルスイッチはトランジスタまたはダイオードで構成することができる。また、

１５）　第１強磁性磁化固着膜、第１トンネル接合膜、第１磁性層、非磁性導電層、第２磁性層、第２トンネル接合膜、及び第２強磁性磁化固着膜は積層形成されている。

１６）　第２及び第３配線は夫々の一端で同一のセンスアンプに接続されている。

１７）　トンネル接合素子及びセルスイッチからなるメモリセルを行方向及び列方向にアレイ状に備る。

１８）　列方向に伸びる第１配線及び行方向に伸びる第２及び第３配線を複数本備える。

１９）　列方向にアレイ状に並ぶ複数のセルトランジスタのゲート電極は一本の配線に共通接続されている。

２０）　行方向にアレイ状に並ぶ複数のトンネル接合素子は、第２及び第３配線に共通接続されている。

２１）　第２及び第３配線はトンネル接合素子を上下から挟み、第２及び第３の配線と交差する磁気書き込み用配線を２本備える。

２２）第２及び第３配線のいずれかとセンスアンプとの間にスイッチを備え、第２及び第３の配線と交差する磁気書き込み用配線を１本備える。

２３）　第１強磁性磁化固着膜及び第２強磁性磁化固着膜のうち、基板主面より最も離れて形成された強磁性磁化固着膜と同一層上に形成され、第１配線と磁気記憶膜を電気的に接続する電極膜を備える。

２４）　非磁性導電層は、Ｃｕ，Ｒｕ，Ｃｒ，Ｒｅ，Ｉｒから選ばれる金属、あるいはＣｕ，Ｒｕ，Ｃｒ，Ｒｅ，Ｉｒを５０ａｔｏｍ％以上含む合金からなる。

【００２５】

【発明の実施の形態】（第１の実施の形態）以下、本発明の磁気メモリ装置の回路構成に関する第１の実施形態を、図１の回路図を用いて説明する。

【００２６】本発明の磁気メモリ装置は、構成する複数のメモリセルの夫々に２つ以上のトンネル接合を備える。第１の実施形態ではトンネル接合を２つ備える２重トンネル接合素子１１を用いて説明するが、これを多重トンネル接合に拡張した形態も本発明に含まれる。

【００２７】図１に示す２重トンネル接合素子１１ａ，１１ｂの構成を１１ａの素子を用いて説明する。素子１１ａは、第１の強磁性磁化固着膜／第１のトンネル絶縁膜／第１磁性層からなるトンネル接合１１ａ－１と、第２の強磁性層／第２のトンネル絶縁膜／第２の強磁性磁化固着膜からなるトンネル接合１１ａ－２を備える。これらが順次積層されると、第１の強磁性磁化固着膜／第１トンネル絶縁膜／第１磁性層／非磁性導電層／第２磁性層／第２トンネル絶縁膜／第２の強磁性磁化固着膜のような積層順となる。

【００２８】第１及び第２強磁性磁化固着膜は、磁化が固定された強磁性膜であり、信号磁界の中でもその磁化は変化しない。第１及び第２磁性層は、間に挿入される非磁性導電層が第１及び第２磁性層の互いの磁化を常に反強磁性結合させる。第１及び第２磁性層、及び非磁性導電層をまとめて磁化記憶膜とするが、信号磁界の印加によって磁化の向きが変わるのは第１及び第２磁性層である。

【００２９】このトンネル接合素子１１ａ，１１ｂの記憶情報の差動検出について、図１のトンネル接合素子１１ａを用いて説明する。情報の記憶は、常に各トンネル接合１１ａ－１，１１ａ－２の一方が低抵抗R_P、他方が高抵抗R_{AP}となるように行う。ここで、低抵抗R_Pは、同じトンネル接合を構成する磁性層と強磁性磁化固着膜の磁化が互いに平行の状態での抵抗であり、高抵抗R_{AP}は強磁性層と強磁性固着膜の磁化が互いに反平行の状態での抵抗である。

【００３０】このトンネル接合１１ａ－１，１１ａ－２に互いに逆方向のトンネル電流を流すと、各接合を流れるトンネル電流値あるいは負荷電圧の差は和として差動検出できる。互いに逆方向のトンネル電流とは、トンネル接合１１ａ－１では、第１の磁性層から第１のトンネル絶縁膜を介して第１の磁性磁化固着膜へ流れ、トンネル接合１１ａ－２では、第２磁性層から第２のトンネル絶縁膜を介して第２の磁性磁化固着膜へ流れる電流である。あるいは、第１の磁性磁化固着膜から第１のトンネル絶縁膜を介して第１磁性層へ、また、第２の磁性磁化固着膜から第２のトンネル絶縁膜を介して第２磁性層へ流れる電流でもよい。

【００３１】この２重トンネル接合素子１１ａは、第１の強磁性磁化固着膜がビット線１３へ、第２の強磁性磁化固着膜がビット線１２へ接続されて共通のセンスアンプ１７に接続されるので、互いに逆方向の電流を流すことにより電流差あるいは負荷電圧差の差動検出が可能になる。

【００３２】記憶膜は図１のトランジスタ１４ａのソース・ドレインに電気接続される。これは、記憶膜を構成する第１磁性層、非磁性導電層、第２磁性層の全て、あ

るいはいずれかが導電層を介してソース・ドレインに電気接続される構成とできる。

【００３３】ビット線１２、１３には２重トンネル接合素子１１ａと同じ構成を持つ他の２重トンネル接合素子、例えば、図１の２重トンネル接合素子１１ｂが素子１１ａと同じ形式で並列接続される。また、その２重トンネル接合素子１１ｂの記憶膜とセルトランジスタ１４ｂとの接続も２重トンネル接合素子１１ａのそれと同様に行う。

【００３４】同じビット線１２，１３に接続されるトンネル接合素子は２個以上複数設けることが可能であり、図１のビット線１２、１３の伸びる方向にアレイ状に配置される。また、図１の同じビット線に接続されるメモリセルのセルトランジスタ１４ａ，１４ｂは、ソース・ドレインの多端がバストランジスタ１５のソース・ドレインに共通接続される。各セルトランジスタのゲートは対応するワード線１６ａ，１６ｂに接続される。この際、図示しないが、ワード線の長さ方向にアレイ状に配置されたメモリセルのセルトランジスタのゲート電極は同一のワード線に共通接続することができる。

【００３５】第１の実施形態では、１トランジスタと２重トンネル接合素子によって１メモリセルを構成して差動方式を実現することができ、参照セルを用いる必要がなくなるとともに、ビットサイズの縮小に大きく寄与でき、メモリ装置の大容量化が可能である。また、セルトランジスタのバラツキの問題を低減できるためノイズを大幅に低減でき、その結果従来のＭＲＡＭに比べ１０倍以上大きなＳ／Ｎ比が得られる。また、２重以上の多重トンネル接合を用いるためＴＭＲのバイアス依存性も小さい。また、記憶膜が反強磁性的に結合した第１及び第２の強磁性層を備えているため反磁界が小さく、メモリセルが小さくなっても小電流で効率的な書き込みが可能であるため消費電力の小さい大容量不揮発メモリを提供できる。

（第２の実施の形態）第２の実施形態では、第１の実施形態において説明した回路を構成するメモリ装置の構造と、磁気情報の書き込み／読み出しについて図２の断面図を用いて説明する。尚、図２のうち、図１と同一の構成には同一の符号を付し、その詳細な説明は省略する。

【００３６】本実施形態の２重トンネル接合素子１１は、第１の強磁性磁化固着膜２１／第１のトンネル絶縁膜２２／第１磁性層２３／非磁性導電層２４／第２磁性層２５／第２のトンネル絶縁膜２６／第２の強磁性磁化固着膜２７が順次積層形成され、第１磁性層２３／非磁性導電層２４／第２磁性層は記憶膜２８を構成する。この素子１１は、第１の強磁性磁化固着膜２１／第１のトンネル絶縁膜２２／第１磁性層２３によって第１のトンネル接合が、第２磁性層２５／第２のトンネル絶縁膜２６／第２の強磁性磁化固着膜２７によって第２のトンネル接合が構成されている。記憶膜２８は３層構造であるが、さらに多層膜とすることも可能である。尚、図２乃至図４、図６及び図７中のハッチング（斜線）を付した箇所は層間絶縁膜である。

【００３７】記憶膜２８を構成する第１及び第２磁性層２３、２５は互いに反強磁性的に磁気結合している。つまり、第１及び第２磁性層２３、２５の磁化は互いに逆向きに保持され、外部磁界によって反転した後も互いの磁化は逆向きに維持される。このような反強磁性的磁気結合は、第１及び第２磁性層２３，２５間へ薄い非磁性導電層２４を挿入することにより実現できる。

【００３８】第１及び第２強磁性層に交換結合を促す非磁性導電層２４の材料は公知のものから選択可能であるが、Ｃｕ，Ｒｕ，Ｃｒ,Ｒｅ，Ｉｒやこれらの一つを５０ａｔｏｍ%以上含む合金などを用いることが望ましい。特に、Ｒｕ，Ｒｅ，Ｉｒは反強磁性交換結合が強く、しかも薄い膜厚で反強磁性交換結合が得られるので好ましい。

【００３９】また、低い電流磁界による磁化反転を促すためには、反強磁性結合した２つの磁性層は互いに磁化の値が異なることが望ましい。そのために、第１及び第２磁性層の膜厚が異なるか、あるいは異なる材料の磁性層を用いることが好ましい。

【００４０】第１及び第２の強磁性磁化固着膜２１、２７の磁化は図２に示すように、互いに同じ方向に固着されており、反強磁性結合した第１及び第２磁性層２３、２５の磁化が図２の“１”の状態から“０”の状態へ反転することで、このメモリセルの記憶情報の変更が行われる。

【００４１】図２の“１”の状態は、第１の強磁性磁化固着膜２１と第１磁性層２３の磁化の向きが互いに反平行であるから第１トンネル接合が高抵抗R_{AP}、第２磁性層２５と第２強磁性磁化固着膜２７の磁化の向きが互いに平行であるから第２のトンネル接合は低抵抗R_Pとなる。これに対し、図２の“０”の状態は、第１の強磁性磁化固着膜２１と第１磁性層２３の磁化の向きが互いに平行であるから第１のトンネル接合は低抵抗R_P、第２磁性層２５と第２強磁性磁化固着膜２７の磁化の向きが互いに反平行であるから第２トンネル接合の抵抗は高抵抗R_{AP}とできる。

【００４２】次に、このような記憶情報の書き込み方法について説明する。情報を記憶させるには、図２のワード線（ＷＬ）２９，３０に信号電流を流すことで行う。ＷＬ２９は、図２の紙面の左右方向に長く伸び、ＷＬ３０は紙面の垂直方向に長く伸びている。この両者に信号電流を流すことでその交点での２重トンネル接合素子１１のみに情報が記憶される。図２に示すように、記憶膜２８はセルトランジスタ１４のソース・ドレイン３１の一方に導電性材料からなるコンタクト柱（配線）を介して接続され、セルトランジスタ１４の他方のソース・ドレイン３１は図１のバストランジスタ１５に接続さ

れる。記憶動作を行う際にはセルトランジスタのゲート３２をオフさせればトンネル接合に電流は流れない。尚、記憶膜２８とソース・ドレイン３１の一方を接続するコンタクト柱は、図２に点線で示すように、紙面より手前あるいは奥に位置し、ビット線１３及びワード線２９と層間絶縁膜を介して交差する。

【００４３】次に、メモリセルの記憶情報を読み出す手段について説明する。図２に示すセルトランジスタ１４のゲート３２をオン状態にすることによって、２重トンネル接合に互いに逆方向のトンネル電流を流し、それに伴う電流または電圧降下をビット線（ＢＬ）１２、１３を経由して図１のセルアンプ１４において差動検出する。信号電圧は上述の“１”，“０”に対応してΔV（$=(R_{AP}-R_P)I_d$）または$-\Delta V$となり、ＴＭＲの大きさそのものを信号として利用できることになる。このため非常に大きなＳ／Ｎ比が得られる。尚、図２の１０はシリコン等の半導体基板を示し、３１はソース・ドレイン電極を示す。

【００４４】また、図１に示す縦に積層した２重トンネル接合はビットサイズの縮小に大きく寄与できる。また、反強磁性結合した２つの磁性層２３、２５に軟磁性層を用いると、保磁力が小さくなるため、磁気情報を書き込むのに必要な磁界が小さく、素子サイズが小さくなっても記憶電流は大きくならず低消費電力型である。

【００４５】さらにまた、第１の実施形態と同様に、参照セルを使用せず、またトランジスタやトンネル接合素子のバラツキを考慮する必要がないのでコストを著しく低減できる。

【００４６】読み出し感度を大きくするためには第１及び第２強磁性磁化固着膜や第１及び第２磁性層の磁性材料に磁気抵抗効果の大きい材料を用いることが望ましい。従って、磁性層２３、２５、強磁性磁化固着膜２１、２７はＣｏ，Ｆｅ，ＣｏＦｅ、ＣｏＮｉ，ＣｏＦｅＮｉ，ＦｅＮｉ合金などの磁性体、およびＮｉＭｎＳｂ、Co_2MnGeなどのハーフメタルなどを用いることができる。ハーフメタルは一方のスピンバンドにエネルギーギャップが存在するのでスピン分極率が大きく、これを用いるとより大きな磁気抵抗効果を得ることができ、結果としてより大きな信号出力が得られる。

【００４７】また、強磁性磁化固着膜２１、２７の磁化を固着する手段には公知の様々な手段を用いることが可能である。例えば、記憶膜２８の磁性層２３，２５の磁化反転に必要な合成磁界よりも抗磁界の高い強磁性材料を強磁性磁化固着膜２１、２７に用いる手段、また、反強磁性膜を強磁性磁化固着膜２１、２７に接触配置させて反強磁性膜と強磁性磁化固着膜との交換結合を利用して強磁性磁化固着膜の磁化を固着する手段、反強磁性膜に替えて硬質磁性膜を接触配置させてその漏洩磁界によって強磁性磁化固着膜２１、２７の磁化を固定する手段等がある。交換結合に用いる反強磁性膜材料としてはＦｅＭｎ，ＩｒＭｎ，ＰｔＭｎなど、通常のスピンバルブＧＭＲで用いられているものを使用することができる。

【００４８】また、トンネル絶縁膜２２、２６としてはAl_2O_3，Ta_2O_5，酸化シリコン，ＭｇＯなど種々の絶縁性非磁性材料を用いることができる。これらの膜厚の好ましい範囲は５オングストロームから３０オングストロームである。

【００４９】さらに、以上説明したような磁気素子用薄膜は分子線エピタキシー（ＭＢＥ）法、各種スパッタ法、蒸着法など通常の薄膜形成装置を用いて作製することができる。また、実施形態に示すような構造は微細加工技術と多層配線技術を用いて作製することができる。

【００５０】（第３の実施の形態）第３の実施形態では、第１及び第２の実施形態において説明した回路を構成するメモリ装置の他の構造と、その磁気情報の書き込み/読み出しについて図３の断面構造と回路の略式図を用いて説明する。図３のうち、図１及び図２と同一の構成については同一の符号を付し、その詳細な説明は省略する。

【００５１】この実施形態では、ビット線１２、１３の一方、図３ではビット線１３とセンスアンプ１７を、トランジスタ３３を介して接続した回路である。これによって図２では２本あったワード線２９、３０の一本を省略できる。すなわち、情報書き込み時にはビット線１２とワード線３４に電流を流し、同時にトランジスタ３３をオフ状態にしておく。これによってビット線１２に流した電流はトンネル接合を流れず書き込み用磁界発生のみの役割を果たす。

【００５２】尚、読み出し時にはトランジスタ３３をオン状態にすることで、２重トンネル接合素子１１の２つのトンネル接合には互いに逆方向のトンネル電流を流すことができ上述の差動検出が可能である。

【００５３】このように、トランジスタ３３の挿入によりワード線を１本省略することができ、配線層の数を減らすことができる。

【００５４】（第４の実施の形態）第４の実施形態では、第１の実施形態において説明した回路を構成するメモリ装置の他の構造と、その磁気情報の書き込み/読み出しについて図４の断面構造と回路の略式図を用いて説明する。尚、図４の中の図１乃至図３と同一の構成については同一の符号を付し、その詳細な説明は省略する。

【００５５】第４の実施形態では、図４に示すように、トランジスタ１４のソース・ドレイン３１の一方と記憶膜２８との接続をビット線１２と磁性電極３５とを介して行う。これは、図２に示す第２のトンネル絶縁膜２６及び第２の強磁性磁化固着膜２７に穴を設け、その穴に絶縁物を埋め込むことにより作成する。また、強磁性電極３５に替えて非磁性導電膜を用いてもよく、この場合には、強磁性磁化固着膜２７の成膜とは別に非磁性導電膜の堆積と加工が必要になる。

【００５６】図４に示すような構成により、磁気情報の書き込み時にはビット線１２とワード線３４に電流を流し、ビット線１３に接続されたスイッチをオフ状態にしておけば２重トンネル接合１１にトンネル電流は流れず、ビット線１２とワード線３４を流れる２つの電流の合成磁界により記憶膜２８への磁気情報の書き込みが可能である。

【００５７】また、記憶情報の読み出しには、図４のトランジスタ３３をオン状態にしてビット線１２、１３に電流が流れるようにしておき、トランジスタ１４をオン状態にすることで、２重トンネル接合１１へ通電することができ、第１の実施形態で説明した各接合へ逆方向電流を流すことが可能になる。

（第５の実施形態）第１乃至第４の実施形態では、メモリセルにトランジスタとトンネル接合素子を用いた場合の構造・回路構成について説明したが、第５の実施形態では、セルトランジスタの代わりにセルダイオードを用いた回路構成について図５の回路図を用いて説明する。尚、図５のうち、図１乃至図４と同一の構成には同一の符号を付し、その詳細な説明は省略する。

【００５８】図５は図１におけるセルトランシスタ１４ａ、１４ｂをダイオード５１ａ，５１ｂで置き換えた場合の電気回路である。但し、ダイオードはセル選択機能がないのでそれを可能にするように図５ではビット線（ＢＬ）１２，１３の一端に選択トランジスタ５５，５６を設けている。この選択トランジスタ５５，５６は各ビット線に一個設ければ良く、各メモリセルにセルトランジスタを設けるのに比べてメモリ装置の大容量化への悪影響は少ない。

【００５９】この回路における読み出し動作は、セルトランジスタ１４がダイオード５１に代わる以外は図１において説明したものと同様であり、詳細な説明は省略する。

【００６０】また、書き込み動作は、図５に示していない磁気情報書き込み用ワード線とＢＬ１２、１３のいずれかに電流を流して行うことができる。ＢＬ１２，１３に流した電流はダイオード５１を用いることでトンネル接合素子１１に流れることなく磁界発生にのみ寄与する。勿論、互いに直交する磁気情報書き込み用ワード線を２本用いてもよい。

（第６の実施の形態）第６の実施形態では、第５の実施形態において説明した回路を構成するメモリセルの構造と、その磁気情報の書き込み・読み出しについて図６の断面構造と回路の略式図を用いて説明する。尚、図６のうち図１乃至図５と同一の構成については、同一の符号を付しその詳細な説明は省略する。

【００６１】図６の例ではダイオード５１は２重トンネル接合素子１１の記憶膜２８の上部に形成されている。ダイオード５１はｐｎ接合ダイオード、金属と半導体との接触を利用するショットキーダイオード、その他の周知のダイオード等を用いることができ、基本的に２つの層の接合において順方向電圧の印加により電流が流れ、逆方向電圧の印加によって電流が流れない特性をもつ。図６では記憶用ＷＬ３４と上部ＢＬ１２に電流を流してその合成磁界を用いて記憶情報の書き込みを行う。このときダイオード５１が存在するために２重トンネル接合素子には電流は流れない。

【００６２】記憶情報の読み出しは図６のダイオード５１と２つのＢＬ１２、１３を選択することで差動検出することが可能である。

（第７の実施の形態）第７の実施形態では、第５の実施形態において説明した回路を構成するメモリ装置の他の構造と、その磁気情報の書き込み・読み出しについて図７の断面構造と回路の略式図を用いて説明する。尚、図７のうち図１乃至図６と同一の構成については、同一の符号を付しその詳細な説明は省略する。

【００６３】図７には２重トンネル接合素子１１の下部にダイオード５１を形成した断面構造を示す。この構造では、下ビット線１３が図７の紙面垂直方向に長く伸び、上下ビット線１２，１３に電流を流して合成磁界を発生させることで記憶膜２８への書き込みを行う。このときやはりダイオード５１があるために２重トンネル接合素子１１には電流が流れない。読み出しはダイオードに接続する図７で紙面垂直方向に伸びるＷＬ５３、またＢＬ１２，１３を選択することで行うことができる。

【００６４】第５乃至第７の実施形態で説明したダイオード５１を用いれば、その抵抗を調整することによって読み出し電流を調整できる。例えばダイオードの抵抗を大きくすれば読み出し電流は小さくなり、結果としてバイアス電圧が小さくなりＴＭＲ効果の低下を抑制できるという大きな利点をもたらす。尚、このようなバイアス電圧の調整はトランジスタをスイッチ素子として用いた第１乃至４の実施形態の場合も同様である。

【００６５】以上説明した第２乃至第４、第６、第７の実施形態では、メモリセル内のトンネル接合素子に各層が基板面の垂直方向に積層形成された２重トンネル接合素子を用いたが、本発明のトンネル接合素子はこれに限られず、種々変更可能である。つまり、２重以上の多重トンネル素子にも適用可能である。また、必ずしも積層形成される必要はなく、本発明の趣旨を逸脱しない範囲で構造の変更が可能である。

【００６６】また、第三の発明において述べたように、２つの１重トンネル接合を用いて、常に一方のトンネル接合が低抵抗R_P、他方のトンネル接合が高抵抗R_{AP}の関係を保つよう構成し、非磁性導電層において分岐する、第１トンネル接合を流れる電流と第２トンネル接合を流れる電流との電流差あるいは負荷電圧差を差動検出する方式の磁気メモリ装置も本発明の範囲内にある。

【００６７】第三の発明の磁気メモリ装置では、メモリセルを非磁性導電層と接続する１つのトランジスタと２

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つのトンネル接合素子によって構成できるので、トランジスタ数を減らすことができ、スイッチ（トランジスタあるいはダイオード）のばらつきの問題と１セルの面積の縮小を実現可能である。また、Ｓ/Ｎ比に優れた特性を備えることができる。

【００６８】第三の発明の磁気メモリ装置を実現する構造としては、非磁性導電層に接続する第１トンネル接合と第２トンネル接合を磁性層間の反強磁性結合がなくなる程度に離間して形成することができる。機能的には、既に述べた第１乃至第７の実施形態と異なり、非磁性導電膜による第１及び第２磁性層の反強磁性結合を用いず、これらの磁性層の磁化反転を独立に制御して、常に一方のトンネル接合が低抵抗R_P、他方のトンネル接合が高抵抗R_{AP}の関係をもたせることで差動検出を実現する。従って、両強磁性層の磁化反転に必要な書き込み線がトンネル接合毎に必要になる。

【００６９】その他、本発明は以上述べた趣旨を逸脱しない範囲で、第１乃至第７の実施形態をもとに様々に変更、組み合わせ可能である。

【００７０】

【発明の効果】本発明の磁気メモリ装置は、１スイッチ（トランジスタやダイオード）と２つのトンネル接合を利用して差動方式を実現することができ、優れたＳ/Ｎ比を実現可能である。また、ビットサイズの縮小に大きく寄与でき、記憶容量の大型化が可能である。また、トランジスタやダイオードのバラツキの問題を低減できるためノイズを大幅に低減できる。

【図面の簡単な説明】

【図１】　本発明の第１の実施形態を説明するための回路図。

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＊【図２】　本発明の第２の実施形態を説明するための断面構造及び一部回路の略式図。

【図３】　本発明の第３の実施形態を説明するための断面構造及び一部回路の略式図。

【図４】　本発明の第４の実施形態を説明するための断面構造及び一部回路の略式図。

【図５】　本発明の第５の実施形態を説明するための回路図。

【図６】　本発明の第６の実施形態を説明するための断面構造及び一部回路の略式図。

【図７】　本発明の第７の実施形態を説明するための断面構造及び一部回路の略式図。

【図８】　本発明の従来の磁気メモリ装置の回路図。

【符号の説明】

１ａ，１ｂ，１１ａ－１，１１ａ－２，１１ｂ－１，１１ｂ－２…トンネル接合素子

２，１２，１３…ビット線

３、１６ａ，１６ｂ…セル選択用ワード線

４ａ，４ｂ，１４ａ，１４ｂ…セルトランジスタ

５，１５…バストランジスタ

６．１７…センスアンプ

７…参照セル用ビット線

８…プレート線

１０…半導体等の基板

２９，３０，３４…書き込み用ワード線

３１…ソース・ドレイン電極

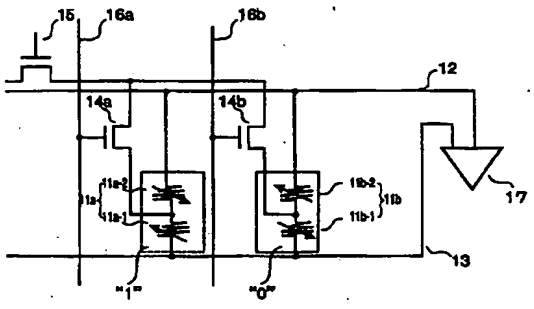
３２…ゲート電極

３３，５５，５６…スイッチトランジスタ

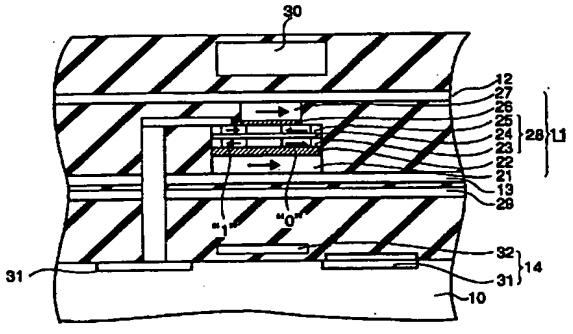
５１，５１ａ，５１ｂ…ダイオード

＊30

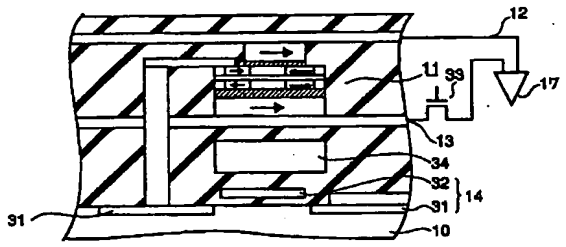
【図１】



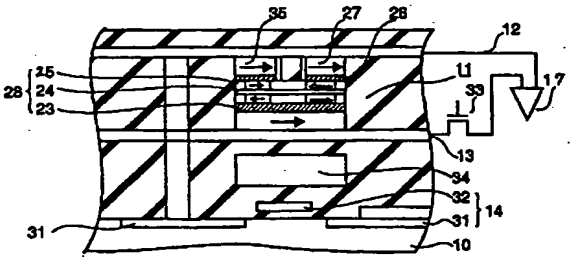
【図２】



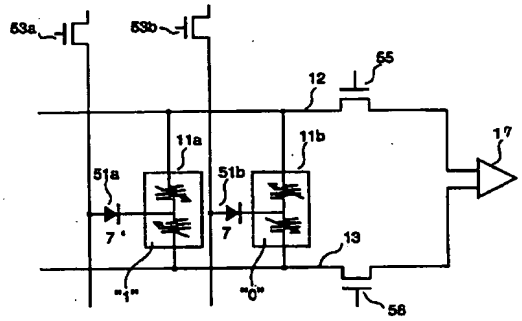
【図３】



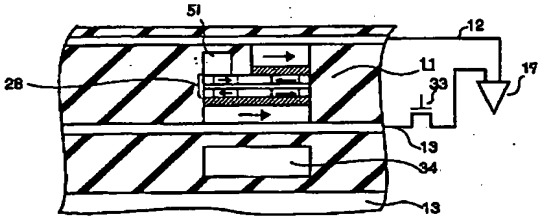
【図４】



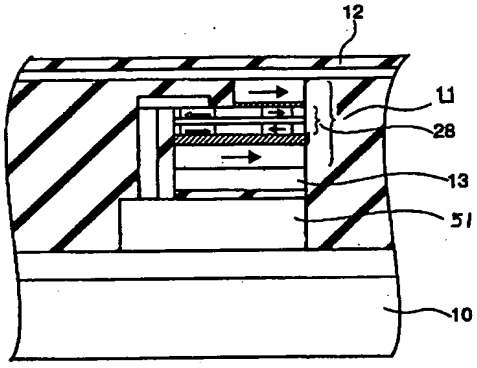
【図５】



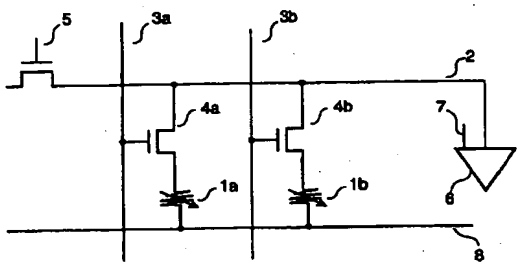
【図６】



【図７】



【図８】



フロントページの続き

(51)Int.Cl.'	識別記号	FI	テーマコード（参考）
H01L 43/08		H01L 43/08	A P Z

(72)発明者　斉藤　好昭
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝研究開発センター内

Ｆターム(参考) 5E049 AA01 AA04 AA07 AA09 AA10
AC00 BA06 DB14 DB20
5F083 FZ10 GA05 GA09 GA12 GA30
MA06 MA19 PR22